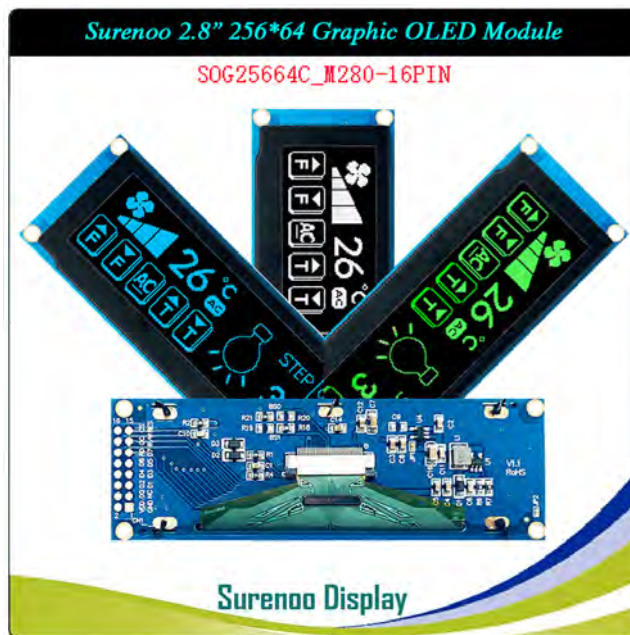


# SURENOO GRAPHIC OLED SERIES DISPLAY

## Product Specification

Part Name: OEL Display Module  
SOG25664C\_M280

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Graphic OLED Display Selection Guide

Graphic OLED Module

Graphic OLED Panel

SSD1322

# 1. Basic Specifications

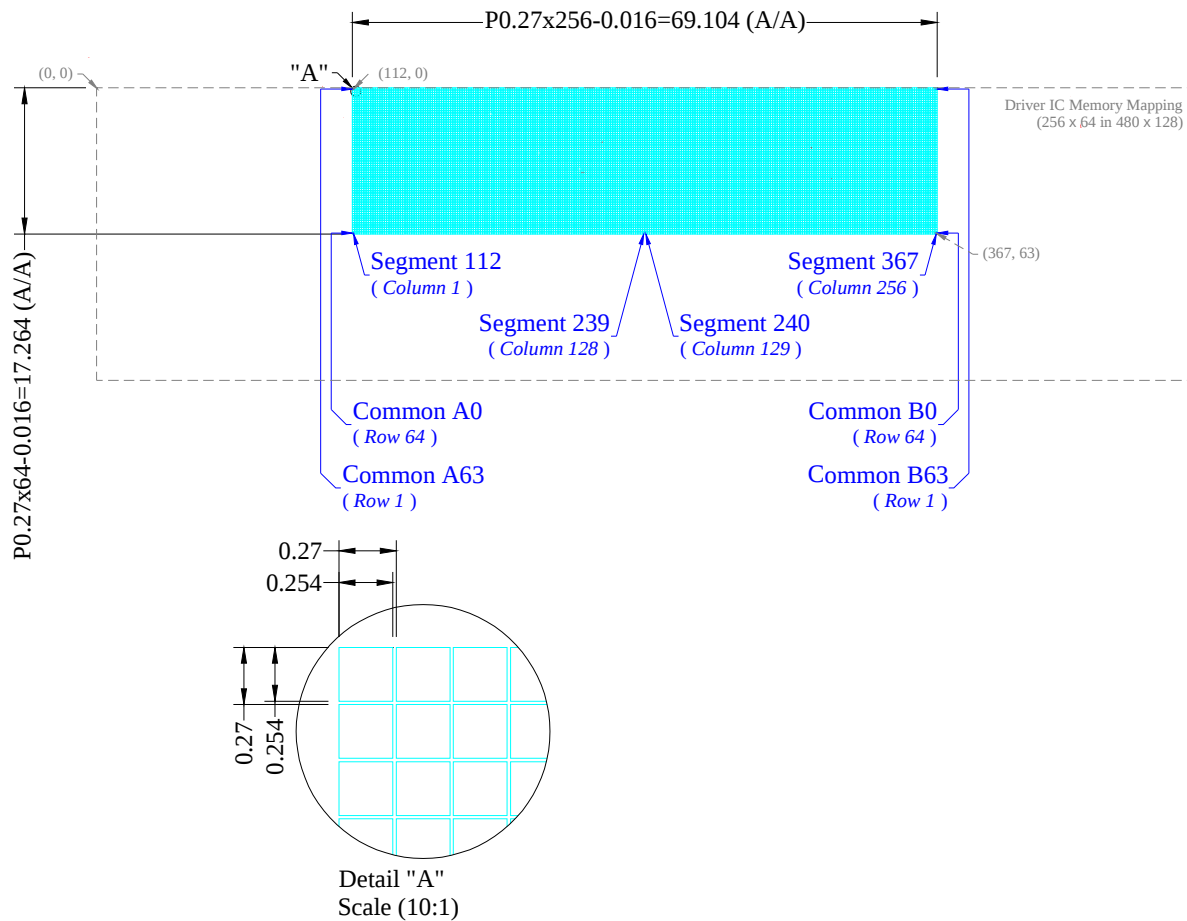
## 1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (Blue)
- 3) Drive Duty: 1/64 Duty

## 1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels:  $256 \times 64$
- 3) PCB Size:  $100.00 \times 35.00 \times 4.8$  (mm)
- 4) Active Area:  $69.10 \times 17.26$  (mm)
- 5) Pixel Pitch:  $0.27 \times 0.27$  (mm)
- 6) Pixel Size:  $0.254 \times 0.254$  (mm)

## 1.3 Active Area / Memory Mapping & Pixel Construction

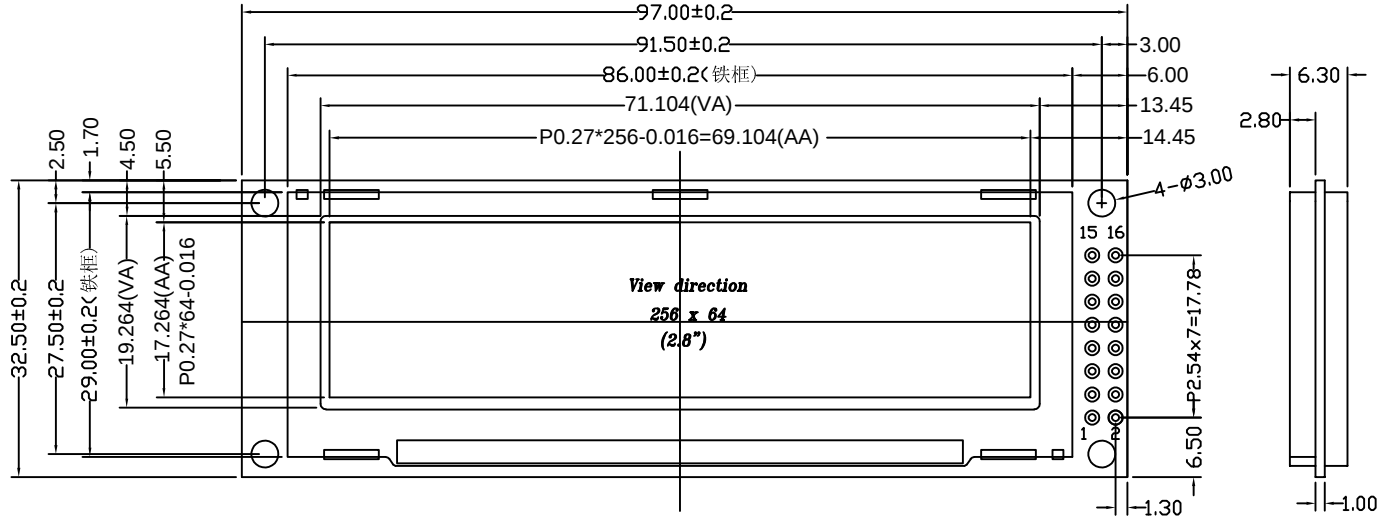




### 3 EXTERNAL DIMENSIONS

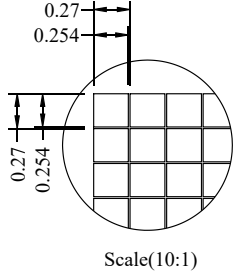
#### NOTES:

1. DISPLAY TYPE: 2.8" 256\*64 OLED Module
2. VIEWING DIRECTION: ALL
3. POLARIZER MODE: TRANSMISSIVE/NORMALLY BLACK
4. DRIVER IC: SSD1322U
5. Resolution: 256x64
6. INTERFACE: 8-bit 68XX/80XX Parallel, 3-/4-wire SPI
7. VOLTAGE: 3.3V
8. OPERATING TEMP: -40°C~70°C



| Item | Date     | Remark           |
|------|----------|------------------|
| A    | 20190425 | Original Drawing |

| Pin Descriptions |         |
|------------------|---------|
| Pin              | Symbol  |
| 1                | GND     |
| 2                | VCC     |
| 3                | NC      |
| 4                | D0(CLK) |
| 5                | D1(DIN) |
| 6                | D2      |
| 7                | D3      |
| 8                | D4      |
| 9                | D5      |
| 10               | D6      |
| 11               | D7      |
| 12               | E/RD    |
| 13               | R/W     |
| 14               | DC      |
| 15               | RES     |
| 16               | CS      |



|                                |                                                                           |           |          |      |            |                       |               |
|--------------------------------|---------------------------------------------------------------------------|-----------|----------|------|------------|-----------------------|---------------|
| Customer Approval<br>Signature | SHENZHEN SURENOO TECHNOLOGY CO.,LTD.<br>深圳市襄诺科技有限公司                       |           |          |      |            | Drawing Number        | Rev.          |
|                                | SOG25664C_M280 PM-OLED Display Module<br>Pixel Number: 256x64, Monochrome |           |          |      |            | Material              |               |
|                                |                                                                           |           |          |      |            | Soda Lime / Polyimide |               |
|                                | Unit<br>mm                                                                | Title     | Drawn    | E.E. | Panel / E. | P.M.                  | Scale         |
| General Roughness<br>Φ         |                                                                           | By<br>HBK |          |      |            |                       | Sheet         |
| Tolerance                      | ±0.3                                                                      | Date      | 20190425 |      |            |                       | Size          |
| Angle                          | ±1                                                                        |           |          |      |            |                       | 1:1 1 of 1 A4 |

## 1.5 Pin Definition

Parallel Interface(8080): (R18,R21- Use; R19,R20- No Use)

| ITEM | SYMBOL  | LEVEL      | FUNCTION                     |
|------|---------|------------|------------------------------|
| 1    | GND     | 0V         | Power Ground                 |
| 2    | VDD     | +3.3~+5.0V | Power Supply For Logic       |
| 3    | NC      | -          | No connect                   |
| 4~11 | D0~D7   | H/L        | Data Bus                     |
| 12   | RD      | H/L        | 8080: Active LOW Read signal |
| 13   | WR      | H/L        | 8080:Active LOW Write signal |
| 14   | D/C(RS) | H/L        | H: Data L: Command           |
| 15   | /RST    | H/L        | Active LOW Reset signal      |
| 16   | /CS     | L          | Chip Select                  |

Parallel Interface(6800): (R18,R20- Use; R19,R21- NO Use)

| ITEM | SYMBOL  | LEVEL      | FUNCTION                                                  |
|------|---------|------------|-----------------------------------------------------------|
| 1    | GND     | 0V         | Power Ground                                              |
| 2    | VDD     | +3.3~+5.0V | Power Supply For Logic                                    |
| 3    | NC      | -          | No connect                                                |
| 4~11 | D0~D7   | H/L        | Data Bus                                                  |
| 12   | RD      | H/L        | 6800:Operation enable signal. Falling edge triggered.     |
| 13   | WR      | H/L        | 6800:Read/Write select signal, R/W=1: Read R/W: =0: Write |
| 14   | D/C(RS) | H/L        | H: Data L: Command                                        |
| 15   | /RST    | H/L        | Active LOW Reset signal                                   |
| 16   | /CS     | L          | Chip Select                                               |

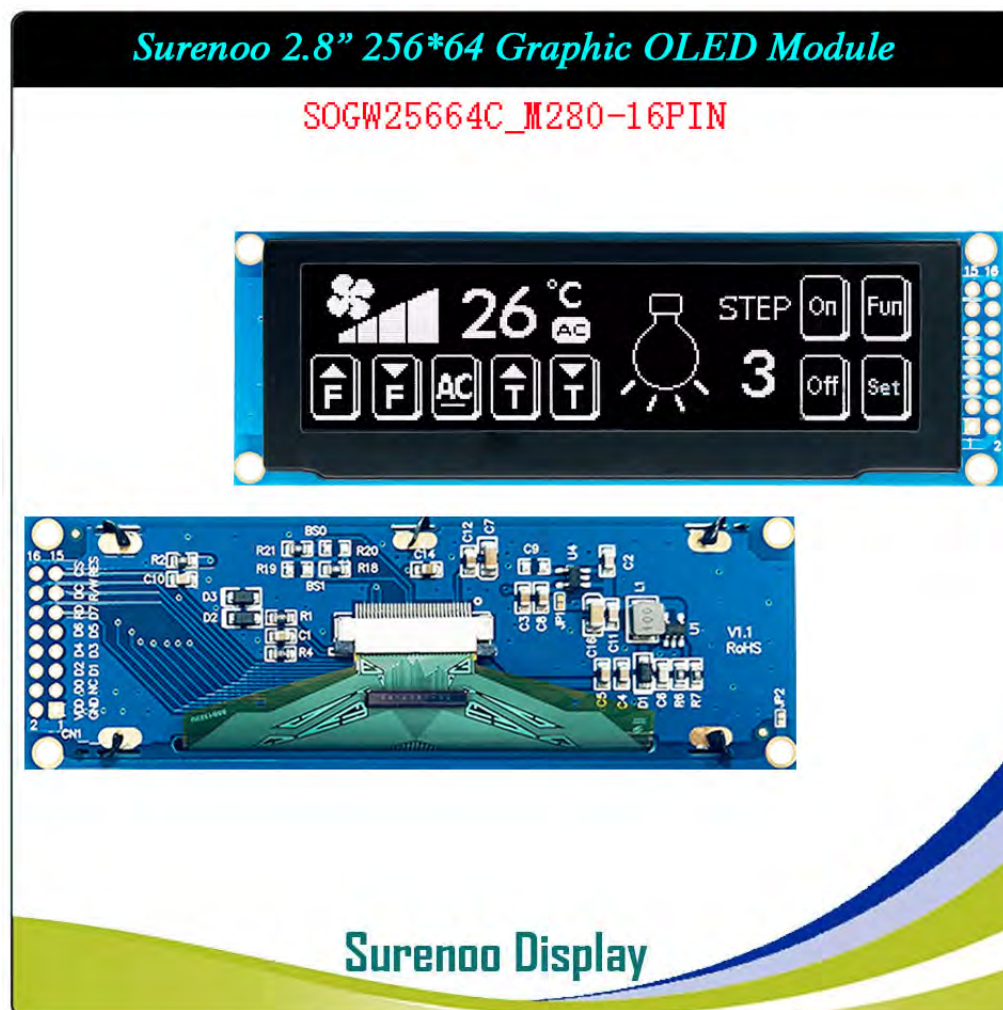
4-SPI: (R19,R21- Use; R18,R20- No Use)

| ITEM | SYMBOL   | LEVEL      | FUNCTION                 |
|------|----------|------------|--------------------------|
| 1    | GND      | 0V         | Power Ground             |
| 2    | VDD      | +3.3~+5.0V | Power Supply For Logic   |
| 3    | NC       | -          | No connect               |
| 4    | SCLK(D0) | H/L        | Serial Clock signal      |
| 5    | SDIN(D1) | H/L        | Serial Data input signal |
| 6    | NC(D2)   | -          | No connect               |
| 7~11 | D3~D7    | 0V         | Power Ground             |
| 12   | RD       | 0V         | Power Ground             |
| 13   | WR       | 0V         | Power Ground             |
| 14   | D/C(RS)  | H/L        | H: Data L: Command       |
| 15   | /RST     | H/L        | Active LOW Reset signal  |
| 16   | /CS      | L          | Chip Select              |

### 3-SPI : (R19,R20- Use; R18,R21 -No Use)

| ITEM | SYMBOL   | LEVEL      | FUNCTION                 |
|------|----------|------------|--------------------------|
| 1    | GND      | 0V         | Power Ground             |
| 2    | VDD      | +3.3~+5.0V | Power Supply For Logic   |
| 3    | NC       | -          | No connect               |
| 4    | SCLK(D0) | H/L        | Serial Clock signal      |
| 5    | SDIN(D1) | H/L        | Serial Data input signal |
| 6    | NC(D2)   | -          | No connect               |
| 7~11 | D3~D7    | 0V         | Power Ground             |
| 12   | RD       | 0V         | Power Ground             |
| 13   | WR       | 0V         | Power Ground             |
| 14   | D/C(RS)  | 0V         | Power Ground             |
| 15   | /RST     | H/L        | Active LOW Reset signal  |
| 16   | /CS      | L          | Chip Select              |

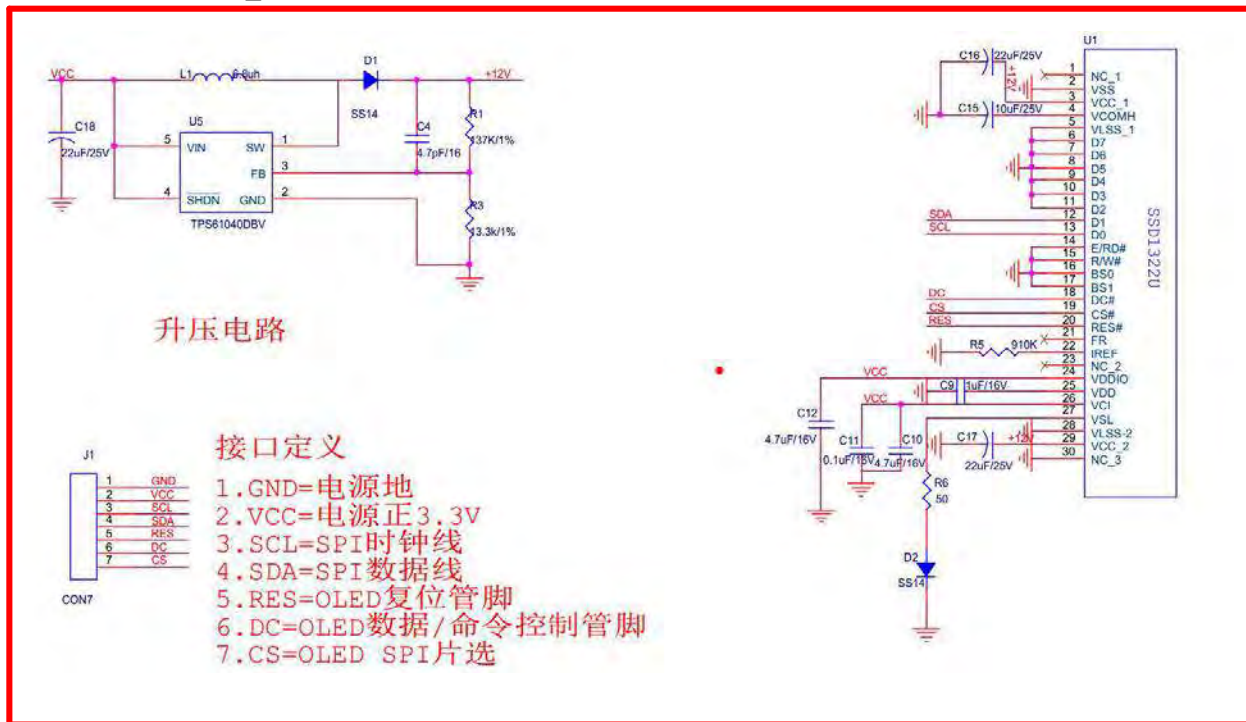
## 1.6 Product Picture





## 1.7 Schematic Diagram

Model: SOG25664C\_M280



## 2. Absolute Maximum Ratings

| Parameter                         | Symbol     | Min    | Max      | Unit | Notes |
|-----------------------------------|------------|--------|----------|------|-------|
| Supply Voltage for Operation      | $V_{CI}$   | -0.3   | 4        | V    | 1, 2  |
| Supply Voltage for Logic          | $V_{DD}$   | -0.5   | 2.75     | V    | 1, 2  |
| Supply Voltage for I/O Pins       | $V_{DDIO}$ | -0.5   | $V_{CI}$ | V    | 1, 2  |
| Supply Voltage for Display        | $V_{CC}$   | -0.5   | 16       | V    | 1, 2  |
| Operating Current for $V_{CC}$    | $I_{CC}$   | -      | 60       | mA   | 1, 2  |
| Operating Temperature             | $T_{OP}$   | -40    | 85       | °C   | 3     |
| Storage Temperature               | $T_{STG}$  | -40    | 90       | °C   | 3     |
| Life Time (80 cd/m <sup>2</sup> ) |            | 10,000 | -        | hour | 4     |
| Life Time (60 cd/m <sup>2</sup> ) |            | 20,000 | -        | hour | 4     |

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4:  $V_{CC} = 12.0V$ ,  $T_a = 25^{\circ}C$ , 50% Checkerboard.

Software configuration follows Section 4.5 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

### 3. Optics & Electrical Characteristics

#### 3.1 Optics Characteristics

| Characteristics    | Symbol     | Conditions  | Min          | Typ          | Max          | Unit              |
|--------------------|------------|-------------|--------------|--------------|--------------|-------------------|
| Brightness         | $L_{br}$   | Note 5      | 60           | 80           | -            | cd/m <sup>2</sup> |
| C.I.E.             | (x)<br>(y) | C.I.E. 1931 | 0.12<br>0.22 | 0.16<br>0.26 | 0.20<br>0.30 |                   |
| Dark Room Contrast | CR         |             | -            | >10,000:1    | -            |                   |
| Viewing Angle      |            |             | -            | Free         | -            | degree            |

\* Optical measurement taken at  $V_{CI} = 2.8V$ ,  $V_{CC} = 12.0V$ .  
Software configuration follows Section 4.4 Initialization.

#### 3.2 DC Characteristics

| Characteristics                                                   | Symbol                      | Conditions           | Min                   | Typ  | Max                   | Unit    |
|-------------------------------------------------------------------|-----------------------------|----------------------|-----------------------|------|-----------------------|---------|
| Supply Voltage for Operation                                      | $V_{CI}$                    |                      | 2.4                   | 2.8  | 3.5                   | V       |
| Supply Voltage for Logic                                          | $V_{DD}$                    |                      | 2.4                   | 2.5  | 2.6                   | V       |
| Supply Voltage for I/O Pins                                       | V                           |                      | 1.65                  | 1.8  | $V_{CI}$              |         |
| Supply Voltage for Display                                        | $V_{CC}$                    | Note 5               | 11.5                  | 12   | 12.5                  |         |
| High Level Input                                                  | V                           |                      | $0.8 \times V_{DDIO}$ | -    | $V_{DDIO}$            | V       |
| Low Level Input                                                   | $V_{IL}$                    |                      | 0                     | -    | $0.2 \times V_{DDIO}$ | V       |
| High Level Output                                                 | $V_{OH}$                    | $I_{out} = 100\mu A$ | $0.9 \times V_{DDIO}$ | -    | $V_{DDIO}$            | V       |
| Low Level Output                                                  | $V_{OL}$                    | $I_{out} = 100\mu A$ | 0                     | -    | $0.1 \times V_{DDIO}$ | V       |
| Operating Current for $V_{CI}$                                    | $I_{CI}$                    |                      | -                     | 180  | 300                   | $\mu A$ |
| Operating Current for $V_{CC}$<br>Sleep Mode Current for $V_{CI}$ | $I_{CC}$<br>$I_{CI, SLEEP}$ | Note 6               |                       | 17.8 | 22.3                  | mA      |
|                                                                   |                             | Note 7               | -                     | 28.1 | 35.1                  | mA      |
|                                                                   |                             | Note 8               | -                     | 47.7 | 59.7                  | mA      |
| Sleep Mode Current for $V_{CC}$                                   | $I_{CC, SLEEP}$             |                      | -                     | 20   | 100                   | $\mu A$ |
| Sleep Mode Current for $V_{CC}$                                   | $I_{CC, SLEEP}$             |                      | -                     | 2    | 10                    | $\mu A$ |

Note 5: Brightness ( $L_{br}$ ) and Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics and the customer's request.

Note 6:  $V_{CI} = 2.8V$ ,  $V_{CC} = 12.0V$ , 30% Display Area Turn on.

Note 7:  $V_{CI} = 2.8V$ ,  $V_{CC} = 12.0V$ , 50% Display Area Turn on.

Note 8:  $V_{CI} = 2.8V$ ,  $V_{CC} = 12.0V$ , 100% Display Area Turn on.

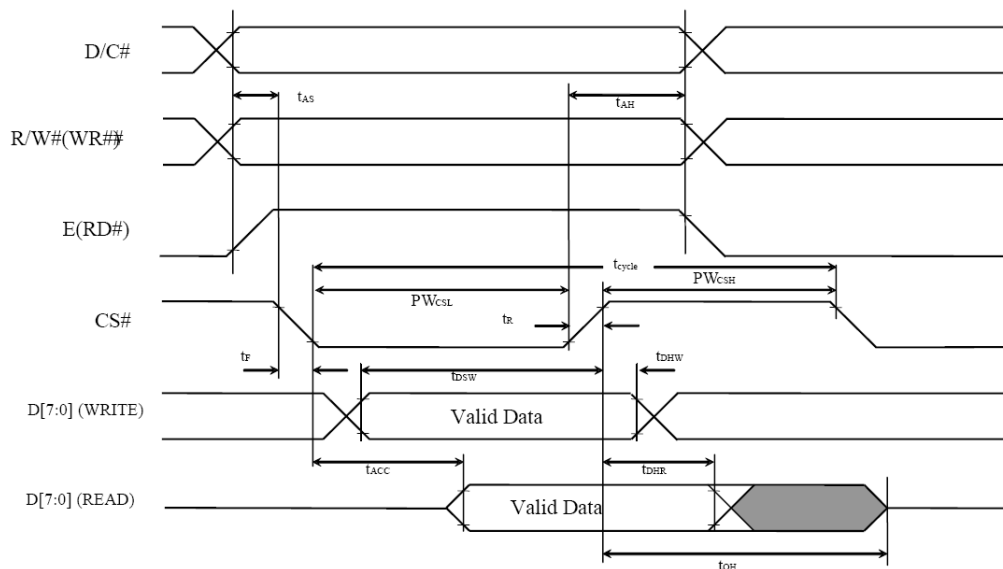
\* Software configuration follows Section 4.4 Initialization.

### 3.3 AC Characteristics

#### 3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol             | Description                          | Min | Max | Unit |
|--------------------|--------------------------------------|-----|-----|------|
| $t_{\text{cycle}}$ | Clock Cycle Time                     | 300 | -   | ns   |
| $t_{\text{AS}}$    | Address Setup Time                   | 10  | -   | ns   |
| $t_{\text{AH}}$    | Address Hold Time                    | 0   | -   | ns   |
| $t_{\text{DSW}}$   | Write Data Setup Time                | 40  | -   | ns   |
| $t_{\text{DHW}}$   | Write Data Hold Time                 | 7   | -   | ns   |
| $t_{\text{DHR}}$   | Read Data Hold Time                  | 20  | -   | ns   |
| $t_{\text{OH}}$    | Output Disable Time                  | -   | 70  | ns   |
| $t_{\text{ACC}}$   | Access Time                          | -   | 140 | ns   |
| $PW_{\text{CSL}}$  | Chip Select Low Pulse Width (Read)   | 120 | -   | ns   |
|                    | Chip Select Low Pulse Width (Write)  | 60  |     |      |
| $PW_{\text{CSH}}$  | Chip Select High Pulse Width (Read)  | 60  | -   | ns   |
|                    | Chip Select High Pulse Width (Write) | 60  |     |      |
| $t_{\text{R}}$     | Rise Time                            | -   | 15  | ns   |
| $t_{\text{F}}$     | Fall Time                            | -   | 15  | ns   |

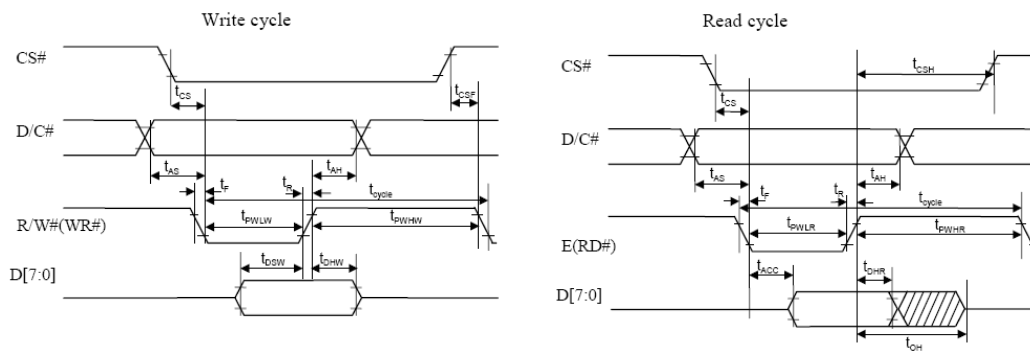
\* ( $V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$ ,  $V_{\text{DDIO}} = 1.6\text{V}$ ,  $V_{\text{CI}} = 2.8\text{V}$ ,  $T = 25^\circ\text{C}$ )



### 3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol             | Description                          | Min | Max | Unit |
|--------------------|--------------------------------------|-----|-----|------|
| $t_{\text{cycle}}$ | Clock Cycle Time                     | 300 | -   | ns   |
| $t_{\text{AS}}$    | Address Setup Time                   | 10  | -   | ns   |
| $t_{\text{AH}}$    | Address Hold Time                    | 0   | -   | ns   |
| $t_{\text{DSW}}$   | Write Data Setup Time                | 40  | -   | ns   |
| $t_{\text{DHW}}$   | Write Data Hold Time                 | 7   | -   | ns   |
| $t_{\text{DHR}}$   | Read Data Hold Time                  | 20  | -   | ns   |
| $t_{\text{OH}}$    | Output Disable Time                  | -   | 70  | ns   |
| $t_{\text{ACC}}$   | Access Time                          | -   | 140 | ns   |
| $t_{\text{PWLRL}}$ | Read Low Time                        | 150 | -   | ns   |
| $t_{\text{PWLW}}$  | Write Low Time                       | 60  | -   | ns   |
| $t_{\text{PWHRL}}$ | Read High Time                       | 60  | -   | ns   |
| $t_{\text{PWHW}}$  | Write High Time                      | 60  | -   | ns   |
| $t_{\text{CS}}$    | Chip Select Setup Time               | 0   | -   | ns   |
| $t_{\text{CSH}}$   | Chip Select Hold Time to Read Signal | 0   | -   | ns   |
| $t_{\text{CSF}}$   | Chip Select Hold Time                | 20  | -   | ns   |
| $t_{\text{R}}$     | Rise Time                            | -   | 15  | ns   |
| $t_{\text{F}}$     | Fall Time                            | -   | 15  | ns   |

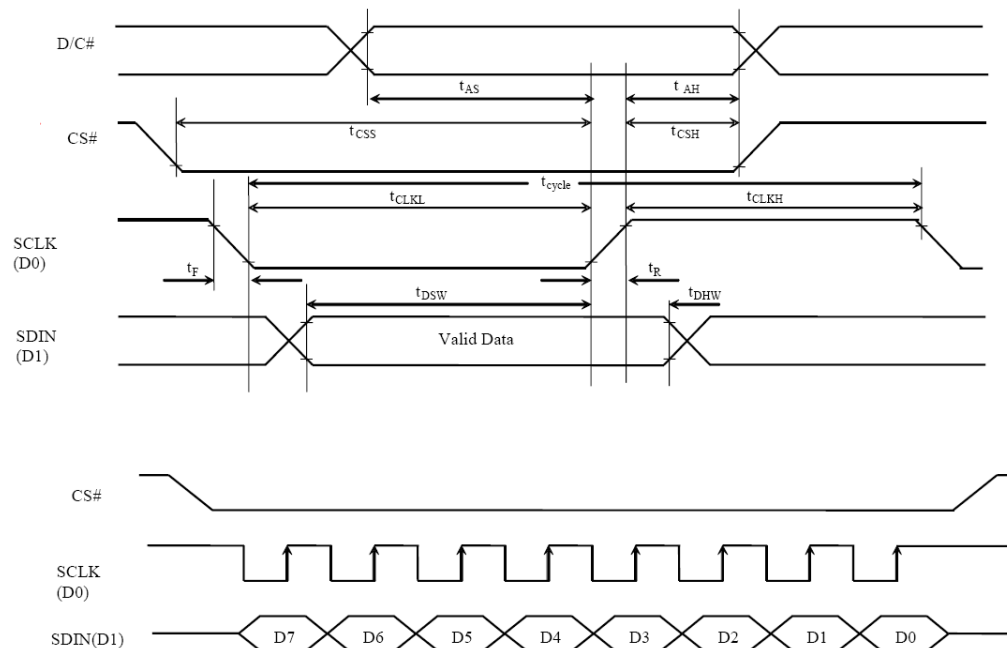
\* ( $V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V}$  to  $2.6\text{V}$ ,  $V_{\text{DDIO}} = 1.6\text{V}$ ,  $V_{\text{CI}} = 2.8\text{V}$ ,  $T_a = 25^\circ\text{C}$ )



### 3.3.3 Serial Interface Timing Characteristics: (4-wire Serial)

| Symbol             | Description            | Min | Max | Unit |
|--------------------|------------------------|-----|-----|------|
| $t_{\text{cycle}}$ | Clock Cycle Time       | 100 | -   | ns   |
| $t_{\text{AS}}$    | Address Setup Time     | 15  | -   | ns   |
| $t_{\text{AH}}$    | Address Hold Time      | 15  | -   | ns   |
| $t_{\text{CSS}}$   | Chip Select Setup Time | 20  | -   | ns   |
| $t_{\text{CSH}}$   | Chip Select Hold Time  | 10  | -   | ns   |
| $t_{\text{DSW}}$   | Write Data Setup Time  | 15  | -   | ns   |
| $t_{\text{DHW}}$   | Write Data Hold Time   | 15  | -   | ns   |
| $t_{\text{CLKL}}$  | Clock Low Time         | 20  | -   | ns   |
| $t_{\text{CLKH}}$  | Clock High Time        | 20  | -   | ns   |
| $t_{\text{R}}$     | Rise Time              | -   | 15  | ns   |
| $t_{\text{F}}$     | Fall Time              | -   | 15  | ns   |

\* ( $V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$ ,  $V_{\text{DDIO}} = 1.6\text{V}$ ,  $V_{\text{CI}} = 2.8\text{V}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )



### 3.3.4 Serial Interface Timing Characteristics: (3-wire Serial)

| Symbol             | Description            | Min | Max | Unit |
|--------------------|------------------------|-----|-----|------|
| $t_{\text{cycle}}$ | Clock Cycle Time       | 100 | -   | ns   |
| $t_{\text{CSS}}$   | Chip Select Setup Time | 20  | -   | ns   |
| $t_{\text{CSH}}$   | Chip Select Hold Time  | 10  | -   | ns   |
| $t_{\text{DSW}}$   | Write Data Setup Time  | 15  | -   | ns   |
| $t_{\text{DHW}}$   | Write Data Hold Time   | 15  | -   | ns   |
| $t_{\text{CLKL}}$  | Clock Low Time         | 20  | -   | ns   |
| $t_{\text{CLKH}}$  | Clock High Time        | 20  | -   | ns   |
| $t_{\text{R}}$     | Rise Time              | -   | 15  | ns   |
| $t_{\text{F}}$     | Fall Time              | -   | 15  | ns   |

\* ( $V_{\text{DD}} - V_{\text{SS}} = 2.4\text{V to } 2.6\text{V}$ ,  $V_{\text{DDIO}} = 1.6\text{V}$ ,  $V_{\text{CI}} = 2.8\text{V}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )

