# SURENOO GRAPHIC OLED SERIES DISPLAY

# Product Specification

## Part Name: OEL Display Module

## SOG25664A_M550

Please click the following image to buy the sample



**Shenzhen Surenoo Technology Co.,Ltd.**
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**Graphic OLED Display Selection Guide**

**Graphic OLED Module** | **Graphic OLED Panel**

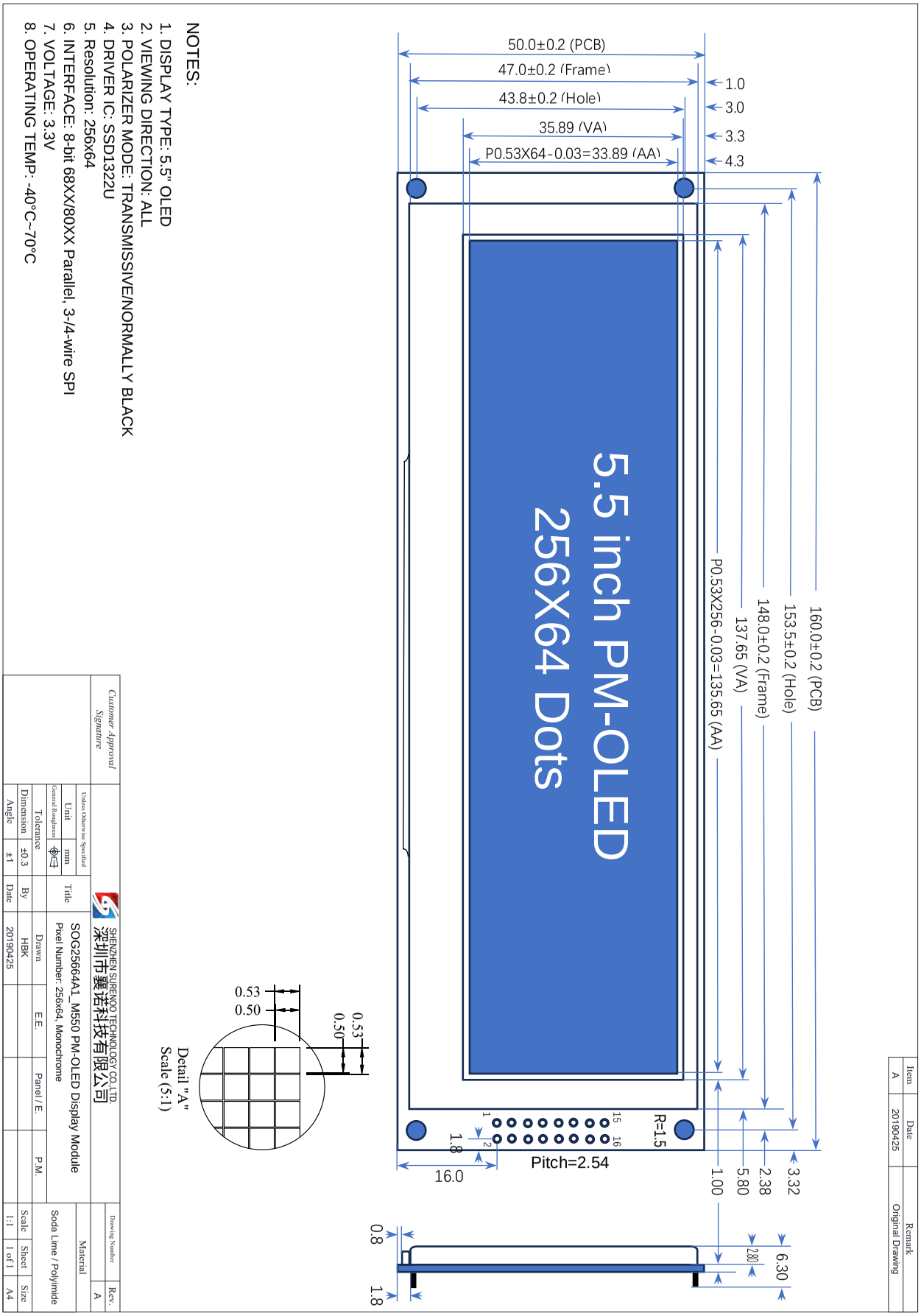
**SSD1322**

# 1. Functions & Features

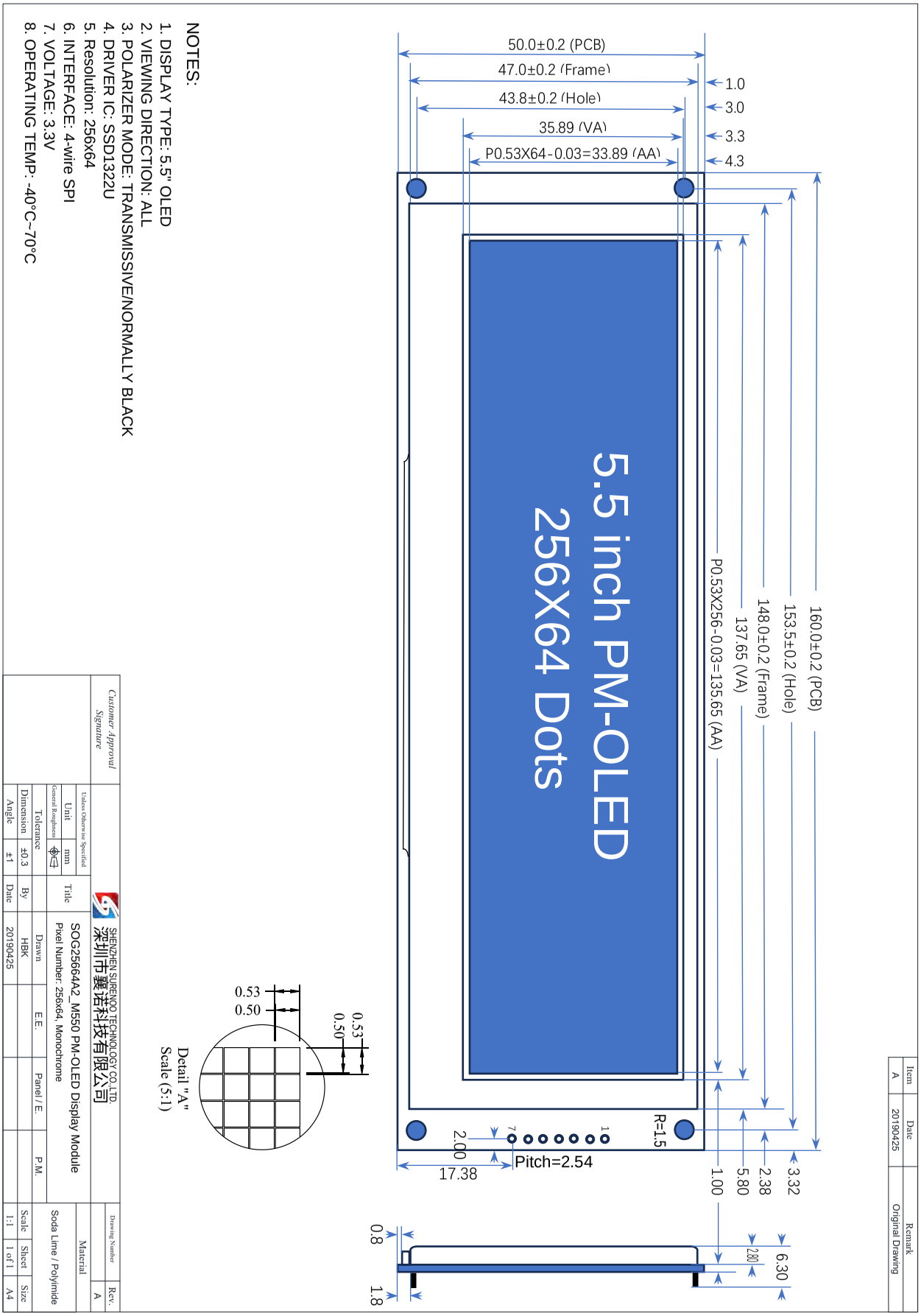
# 2. Mechanical Specifications

| | |
|---|---|
| **Gross Weight** | 0.080Kg |
| **Manufacturer** | Surenoo |
| **Display Type** | Graphic OLED Module |
| **Continuity Supply** | More than 10 years |
| **Part No.** | SOG25664A1_M550 |
| **Diagonal Size (Visual Area)** | 5.5" Inch |
| **Display Format** | 256*64 Dots |
| **Interface** | OLED Module: SOG25664A1_M550, 6800/8080 8-Bit Parallel, 3-/4- Wire Serial SPI (16Pin/2.54 Pin Header) |
| | OLED Module: SOG25664A2_M550, 4-Wire SPI (7Pin/2.54 Pin Header) |
| **IC or Equivalent** | SSD1322 or Equal |
| **Voltage(Type)** | 3.3V |
| **Outline Dimension** | 160.00(W)x50.00(H)x6.30(T)mm |
| **Visual Area** | 137.65x35.890mm |
| **Active Area** | 135.65x33.89mm |
| **Dots Size** | 0.50x0.50mm |
| **Dots Pitch** | 0.53x0.53mm |
| **Display Type** | PM-OLED Panel |
| **Colors Code** | Yellow(SOGY) / Green(SOGG) |
| **IC Package** | COG |
| **Viewing Direction** | Full Viewing Angle |
| **Operating Temperature** | -40℃~70℃ |
| **Storage Temperature** | -40℃~80℃ |

# 3.1 External Dimensions SOG25664A1_M550



# 3.2 External Dimensions SOG25664A2_M550



# 4. Pin Description

1 OLED Module: SOG25664A1 M550-16Pin

| Pin No. | Pin Name | | Description | |
|---|---|---|---|---|
| **Parallel Interface(8080): (R18, R21 USE; R19, R20 NO USE) / Parallel Interface(6800): (R18, R20 USE; R19, R21 NO USE)** | | | | |
| 1 | GND | | Ground 0V | |
| 2 | VDD | | Power Supply for logic (3.3V) | |
| 3 | NC | | No connect | |
| 4-11 | D0-D7 | | Data Bus | |
| 12 | 8080: RD | 6800: E | 8080: Active LOW Read signal | 6800: Operation enable signal. Falling edge triggered. |
| 13 | 8080: WR | 6800: R/W | 8080: Active LOW Writed signal | 6800: Read/Write: R/W=1: Read; R/W:=0: Write |
| 14 | D/C (RS) | | H: Data; L: Command | |
| 15 | /RST | | Active LOW Reset signal | |
| 16 | /CS | | Chip Selection | |
| **4-SPI: (R19, R21 USE; R18, R20 NO USE) / 3-SPI : (R19, R20 USE; R18, R21 NO USE)** | | | | |
| 1 | GND | | Ground 0V | |
| 2 | VDD | | Power Supply for logic (3.3V) | |
| 3 | NC | | No connect | |
| 4 | SCLK (D0) | | Serial Clock signal | |
| 5 | SDIN (D1) | | Serial Data Input signal | |
| 6 | NC (D2) | | No connect | |
| 7-13 | GND | | Ground 0V | |
| 14 | 4-SPI: D/C(RS) | 3-SPI: GND | 4-SPI: H: Data; L: Command | 3-SPI: GND |
| 15 | /RST | | Active LOW Reset signal | |
| 16 | /CS | | Chip Selection | |

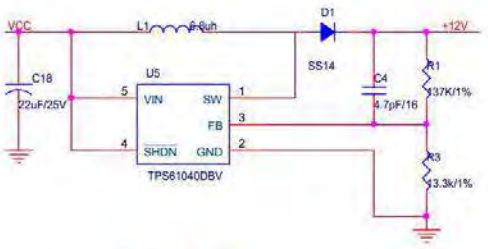
MCU Interface assignment under different bus interface mode:

| Pin Name / Bus Interface | Data/Command Interface | | | | | | | | Control Signal | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | R/W# | CS# | D/C# | RES# |
| 8-bit 8080 | D[7:0] | | | | | | | | RD# | WR# | CS# | D/C# | RES# |
| 8-bit 6800 | D[7:0] | | | | | | | | E | R/W# | CS# | D/C# | RES# |
| 3-wire SPI | Tie LOW | | | | | NC | SDIN | SCLK | Tie LOW | | CS# | Tie LOW | RES# |
| 4-wire SPI | Tie LOW | | | | | NC | SDIN | SCLK | Tie LOW | | CS# | D/C# | RES# |

2. OLED Module: SOG25664A2_M550-7Pin

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | GND | Ground 0V |
| 2 | VDD | Power Supply for logic (3.3V) |
| 3 | SCL | Serial Clock signal |
| 4 | SDA | Serial Data Input signal |
| 5 | /RST | Active LOW Reset signal |
| 6 | D/C | H: Data; L: Command |
| 7 | /CS | Chip Selection |

# 5. Schematic diagram(for reference only)(A2)

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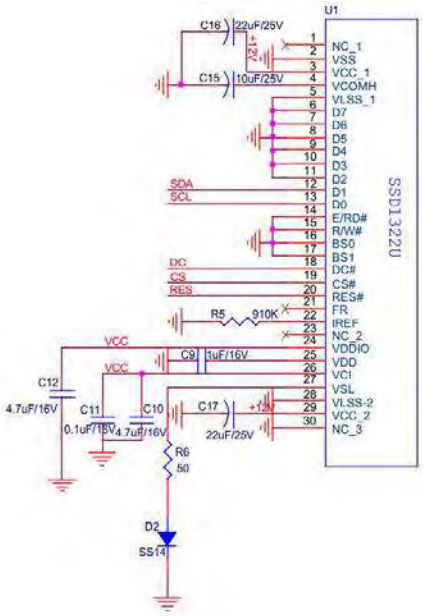
接口定义

1.GND=电源地
2.VCC=电源正3.3V
3.SCL=SPI时钟线
4.SDA=SPI数据线
5.RES=OLED复位管脚
6.DC=OLED数据/命令控制管脚
7.CS=OLED SPI片选




# 6. Maximum Ratings

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply Voltage for Operation | $V_{CI}$ | -0.3 | 4 | V | 1, 2 |
| Supply Voltage for Logic | $V_{DD}$ | -0.5 | 2.75 | V | 1, 2 |
| Supply Voltage for I/O Pins | $V_{DDIO}$ | -0.5 | $V_{CI}$ | V | 1, 2 |
| Supply Voltage for Display | $V_{CC}$ | -0.5 | 16 | V | 1, 2 |
| Operating Current for $V_{CC}$ | $I_{CC}$ | - | 60 | mA | 1, 2 |
| Operating Temperature | $T_{OP}$ | -30 | 70 | ℃ | 3 |
| Storage Temperature | $T_{STG}$ | -40 | 80 | ℃ | 3 |
| Life Time (80 cd/m$^2$) | | 40,000 | - | hour | 4 |

Note 1: All the above voltages are on the basis of "$V_{SS}$ = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: $V_{CC}$ = 12.0V, $T_a$ = 25°C, 50% Checkerboard.
Software configuration follows Section 4.2 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

# 7. Electrical Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage for Operation | $V_{CI}$ | | 2.4 | 2.8 | 3.5 | V |
| Supply Voltage for Logic | $V_{DD}$ | | 2.4 | 2.5 | 2.6 | V |
| Supply Voltage for I/O Pins | $V_{DDIO}$ | | 1.65 | 1.8 | $V_{CI}$ | V |
| Supply Voltage for Display | $V_{CC}$ | Note 3 | 14.5 | 15 | 15.5 | V |
| High Level Input | $V_{IH}$ | | 0.8×$V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low Level Input | $V_{IL}$ | | 0 | - | 0.2×$V_{DDIO}$ | V |
| High Level Output | $V_{OH}$ | $I_{out}$ = 100μA, 3.3MHz | 0.9×$V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low Level Output | $V_{OL}$ | $I_{out}$ = 100μA, 3.3MHz | 0 | - | 0.1×$V_{DDIO}$ | V |
| Operating Current for $V_{CI}$ | $I_{CI}$ | | - | 1.8 | 2.25 | mA |
| Operating Current for $V_{CC}$ | $I_{CC}$ | Note 4 | - | 39.8 | 49.8 | mA |
| | | Note 5 | - | 64.0 | 80.0 | mA |

# 8. Optics Characteristic

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Brightness | $L_{br}$ | With Polarizer (Note 3) | 60 | 80 | - | cd/m$^2$ |
| C.I.E. (Green) | (x)<br>(y) | Without Polarizer | 0.27<br>0.58 | 0.31<br>0.62 | 0.35<br>0.66 | |
| Dark Room Contrast | CR | | - | >2000:1 | - | |
| View Angle | | | >160 | - | - | degree |

* Optical measurement taken at $V_{CI}$ = 2.8V, $V_{CC}$ = 15V.
Software configuration follows Section 4.2 Initialization.

| | | | | | | |
|---|---|---|---|---|---|---|
| Sleep Mode Current for $V_{CI}$ | $I_{CI, SLEEP}$ | | - | 1 | 5 | μA |
| Sleep Mode Current for $V_{CC}$ | $I_{CC, SLEEP}$ | | - | 1 | 5 | μA |

Note 3: Brightness ($L_{br}$) and Supply Voltage for Display ($V_{CC}$) are subject to the change of the panel characteristics and the customer's request.
Note 4: $V_{CI}$ = 2.8V, $V_{CC}$ = 15V, 50% Display Area Turn on.
Note 5: $V_{CI}$ = 2.8V, $V_{CC}$ = 15V, 100% Display Area Turn on.

* Software configuration follows Section 4 4 Initialization

# 9. Timing Characteristics(4-SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

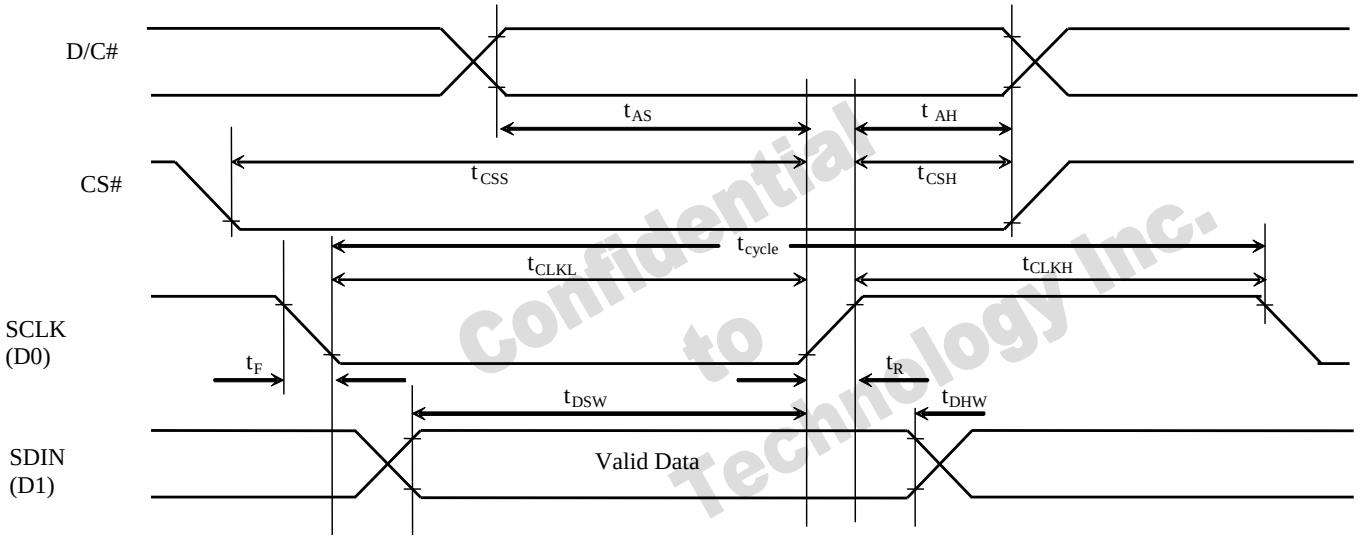
**Table 8-4 : Control pins of 4-wire Serial interface**

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---|---|---|---|---|---|
| Write command | Tie LOW | Tie LOW | L | L | ↑ |
| Write data | Tie LOW | Tie LOW | L | H | ↑ |

**Note**
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

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($V_{DD}$ - $V_{SS}$ = 2.4 to 2.6V, $V_{DDIO}$=1.6V, $V_{CI}$ = 3.3V, $T_A$ = 25°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 15 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 15 | - | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 20 | - | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 10 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 15 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | - | ns |
| $t_{CLKL}$ | Clock Low Time | 20 | - | - | ns |
| $t_{CLKH}$ | Clock High Time | 20 | - | - | ns |
| $t_R$ | Rise Time | - | - | 15 | ns |
| $t_F$ | Fall Time | - | - | 15 | ns |

# 10. Commands

Refer to the Technical Manual for the SSD1322U

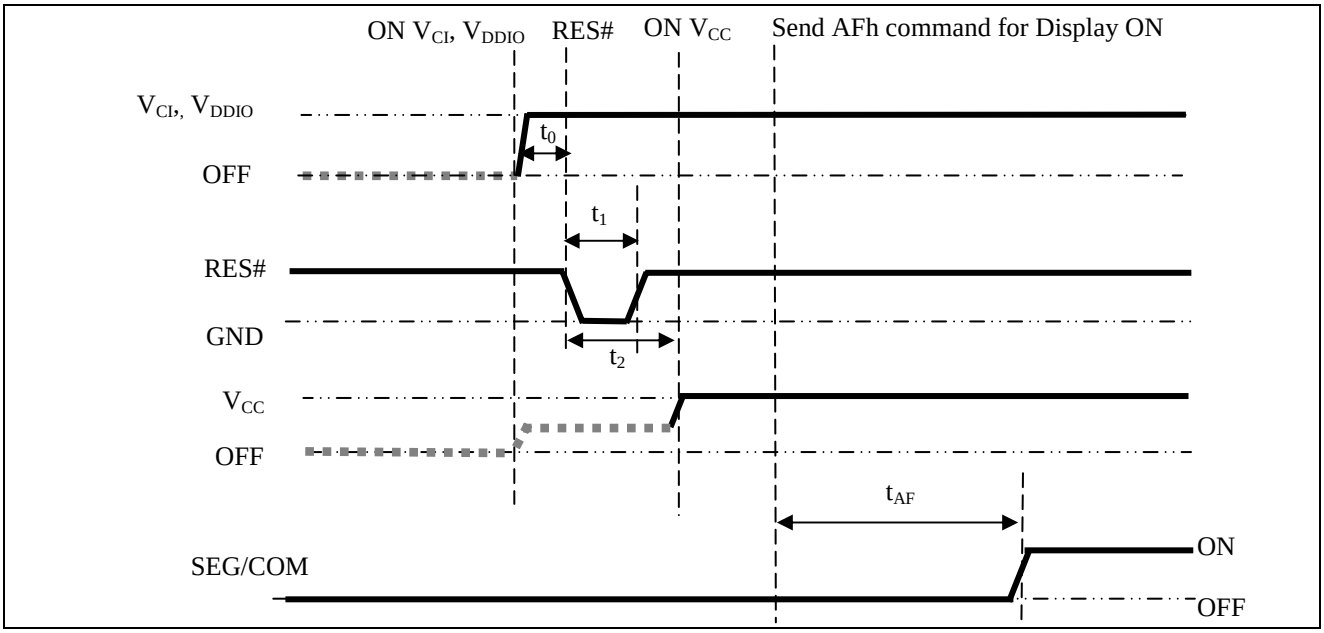
# 11. Power ON an OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1322 (assume $V_{CI}$ and $V_{DDIO}$ are at the same voltage level and internal $V_{DD}$ is used).

*Power ON sequence*:

1. Power ON $V_{CI,}$ $V_{DDIO.}$
2. After $V_{CI}$, $V_{DDIO}$ become stable, set wait time at least 1ms ($t_0$) for internal $V_{DD}$ become stable. Then set RES# pin LOW (logic low) for at least 100us ($t_1$) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us ($t_2$). Then Power ON $V_{CC.}$ (1)
4. After $V_{CC}$ become stable, send command AFh for display ON. SEG/COM will be ON after 200ms ($t_{AF}$).

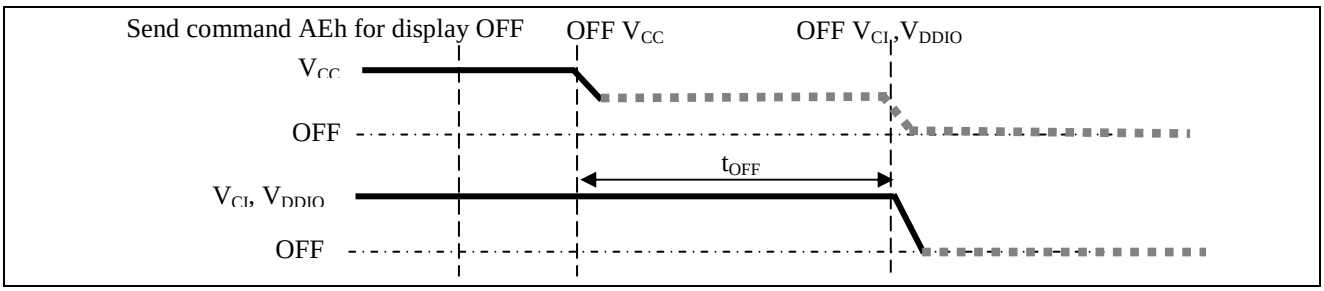
**The Power ON sequence.**




*Power OFF sequence*:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC.}$ (1), (2)
3. Wait for $t_{OFF}$. Power OFF $V_{CI,}$ $V_{DDIO.}$ (where Minimum $t_{OFF}$=0ms (3), Typical $t_{OFF}$=100ms)

**The Power OFF sequence**



**Note:**

(1) Since an ESD protection circuit is connected between $V_{CI}$, $V_{DDIO}$ and $V_{CC}$, $V_{CC}$ becomes lower than $V_{CI}$ whenever $V_{CI}$, $V_{DDIO}$ is ON and $V_{CC}$ is OFF as shown in the dotted line of $V_{CC}$ in Figure 8-14 and Figure 8-15.

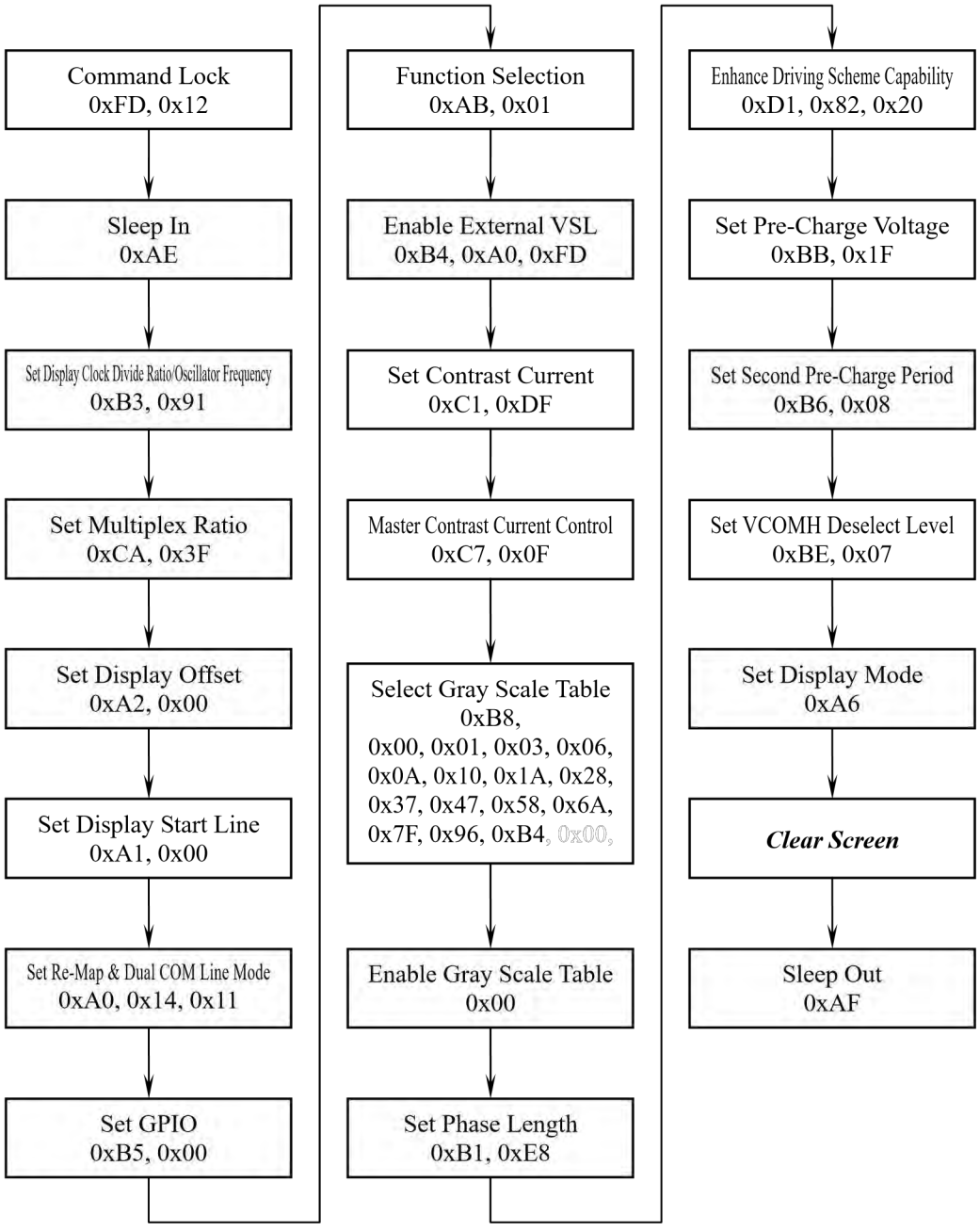
(2) $V_{CC}$ should be kept float (disable) when it is OFF.

(3) $V_{CI}$, $V_{DDIO}$ should not be Power OFF before $V_{CC}$ Power OFF.

(4) The register values are reset after $t_1$.

(5) Power pins ($V_{DD}$, $V_{CC}$) can never be pulled to ground under any circumstance.

# 12. Actual Application Example



# 13. Reliability & Inspection Standards

## 13.1 Test Condition

| Item | Conditions | Criteria |
|---|---|---|
| High Temperature Operation | 70°C, 240 hrs | The operational functions work. |
| Low Temperature Operation | -40°C, 240 hrs | |
| High Temperature Storage | 85°C, 240 hrs | |
| Low Temperature Storage | -40°C, 240 hrs | |
| High Temperature/Humidity Operation | 60°C, 90% RH, 120 hrs | |
| Thermal Shock | -40°C ⇔ 85°C, 24 cycles<br>60 mins dwell | |

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

## Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

## 13.2 Outgoing Quality Control Specifications

### Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

| | |
|---|---|
| Temperature: | 23 ± 5°C |
| Humidity: | 55 ± 15% RH |
| Fluorescent Lamp: | 30W |
| Distance between the Panel & Lamp: | ≥ 50cm |
| Distance between the Panel & Eyes of the Inspector: | ≥ 30cm |

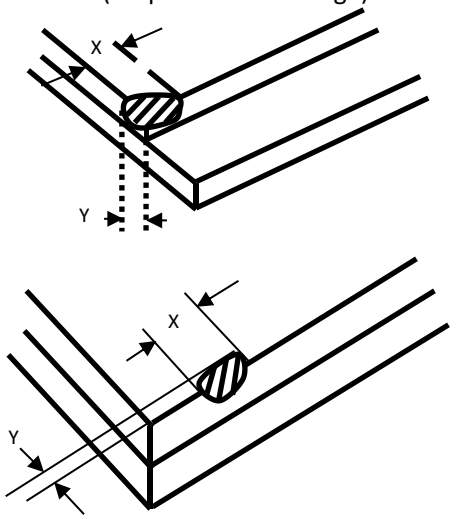
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

## 13.3 AQL(Acceptable Quality Level)

AQL of major and minor defect.

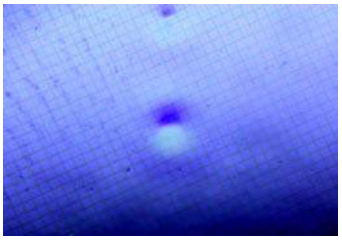
| | MAJOR DEFECT | MINOR DEFECT |
|---|---|---|
| AQL | 0.65 | 1.0 |

**Cosmetic Check (Display Off) in Non-Active Area**

| Check Item | Classification | Criteria |
|---|---|---|
| Panel General Chipping | Minor | X > 6 mm (Along with Edge)<br>Y > 1 mm (Perpendicular to edge)<br>  |

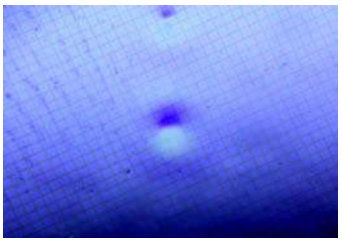
**Cosmetic Check (Display Off) in Active Area**

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

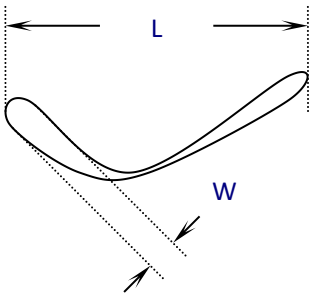
| Check Item | Classification | Criteria |
|---|---|---|
| Any Dirt & Scratch on Polarizer's Protective Film | Acceptable | Ignore for not Affect the Polarizer |
| Scratches, Fiber, Line-Shape Defect (On Polarizer) | Minor | W ≤ 0.1 Ignore<br>W > 0.1<br>L ≤ 2 n ≤ 1<br>L > 2 n = 0 |
| Dirt, Black Spot, Foreign Material, (On Polarizer) | Minor | Φ ≤ 0.1 Ignore<br>0.1 < Φ ≤ 0.25 n ≤ 1<br>0.25 < Φ n = 0 |
| Dent, Bubbles, White spot (Any Transparent Spot on Polarizer) | Minor | Φ ≤ 0.5<br>➔ Ignore if no Influence on Display<br>0.5 < Φ n = 0<br>  |
| Fingerprint, Flow Mark (On Polarizer) | Minor | Not Allowable |

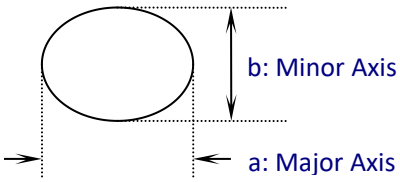
**Cosmetic Check (Display Off) in Active Area**

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

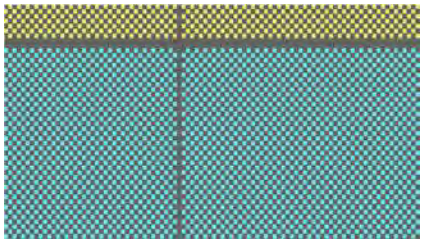
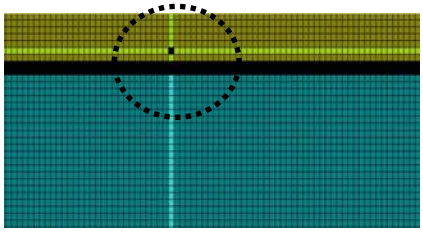
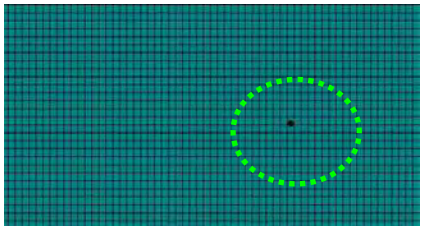
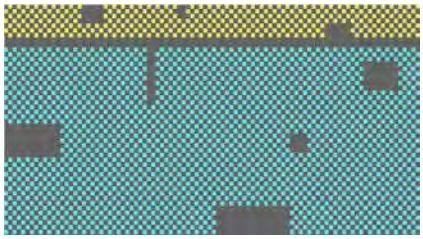
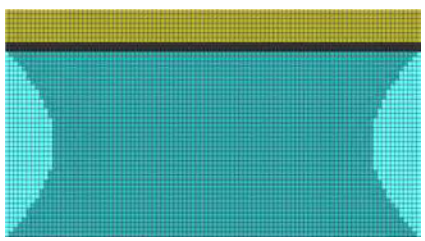
| Check Item | Classification | Criteria |
|---|---|---|
| Any Dirt & Scratch on Polarizer's Protective Film | Acceptable | Ignore for not Affect the Polarizer |
| Scratches, Fiber, Line-Shape Defect (On Polarizer) | Minor | W ≤ 0.1 Ignore<br>W > 0.1<br>L ≤ 2 n ≤ 1<br>L > 2 n = 0 |
| Dirt, Black Spot, Foreign Material, (On Polarizer) | Minor | Φ ≤ 0.1 Ignore<br>0.1 < Φ ≤ 0.25 n ≤ 1<br>0.25 < Φ n = 0 |
| Dent, Bubbles, White spot (Any Transparent Spot on Polarizer) | Minor | Φ ≤ 0.5<br>➔ Ignore if no Influence on Display<br>0.5 < Φ n = 0<br>  |
| Fingerprint, Flow Mark (On Polarizer) | Minor | Not Allowable |

* Protective film should not be tear off when cosmetic check.
** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



**Pattern Check (Display On) in Active Area**

| Check Item | Classification | Criteria |
|---|---|---|
| No Display | Major |  |
| Missing Line | Major |  |
| Pixel Short | Major |  |
| Darker Pixel | Major |  |
| Wrong Display | Major |  |
| Un-uniform | Major |  |

# 14. Precautions

## 14.1 Handing precautions

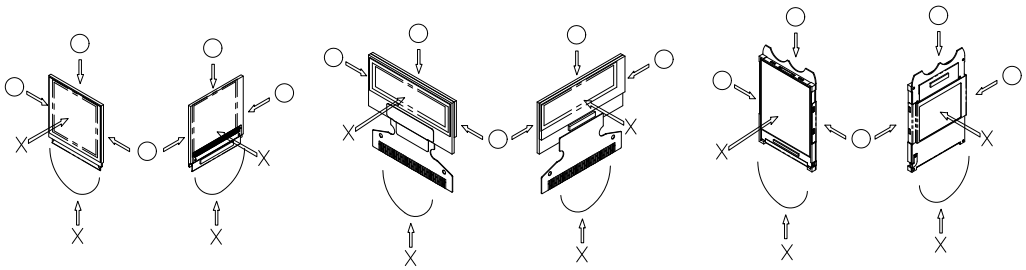
1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

Also, pay attention that the following liquid and solvent may spoil the polarizer:

* Water
* Ketone
* Aromatic Solvents

6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.

9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

## 14.2 Designing precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the $V_{IL}$ and $V_{IH}$ specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit ($V_{DD}$). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1322

* Connection (contact) to any other potential than the above may lead to rupture of the IC.

# 15. The Appendix SSD1322U_Initial code

```
void OLED_Init(void)
{
  //OLED 复位
  OLED_RES_Clr();//RES 置 0
   delay_ms(200);//延时 200ms
   OLED_RES_Set();//RES 置 1

  //OLED 初始化
    OLED_WR_REG(0xae); //Sleep In

    OLED_WR_REG(0xfd);   /*Command Lock*/
    OLED_WR_Byte(0x12);

    OLED_WR_REG(0xb3);     //Set Display Clock Divide Ratio/Oscillator Frequency
    OLED_WR_Byte(0x91);

    OLED_WR_REG(0xca);     //Set Multiplex Ratio
    OLED_WR_Byte(0x3f);

    OLED_WR_REG(0xa2);     //Set Display Offset
    OLED_WR_Byte(0x00);    //

    OLED_WR_REG(0xa1);     //Set Display Start Line
    OLED_WR_Byte(0x00);    //

    OLED_WR_REG(0xa0);     //Set Re-Map $ Dual COM Line Mode
    OLED_WR_Byte(0x06);

    OLED_WR_REG(0xB5);     //Set GPIO
    OLED_WR_Byte(0x00);

    OLED_WR_REG(0xab);     //Function Selection
    OLED_WR_Byte(0x01);    //

    OLED_WR_REG(0xb4);     //Enable External VSL
    OLED_WR_Byte(0xa0);    //
   OLED_WR_Byte(0xf8);     //

   OLED_WR_REG(0xc1);      //Set Contrast Current
   OLED_WR_Byte(0xef);

   OLED_WR_REG(0xc7);      //Master Contrast Current Control
   OLED_WR_Byte(0xff);     //
```

```
OLED_WR_REG(0xB8); //        // Set Gray Scale Table
OLED_WR_Byte(0x0C); //
OLED_WR_Byte(0x18); //
OLED_WR_Byte(0x24); //
OLED_WR_Byte(0x30); //
OLED_WR_Byte(0x3C); //
OLED_WR_Byte(0x48); //
OLED_WR_Byte(0x54); //
OLED_WR_Byte(0x60); //
OLED_WR_Byte(0x6C); //
OLED_WR_Byte(0x78); //
OLED_WR_Byte(0x84); //
OLED_WR_Byte(0x90); //
OLED_WR_Byte(0x9C); //
OLED_WR_Byte(0xA8); //
OLED_WR_Byte(0xB4); //
OLED_WR_REG(0x00);     // Enable Gray Scale Table

OLED_WR_REG(0xb1);     //Set Phase Length
OLED_WR_Byte(0xe2);

OLED_WR_REG(0xd1);     //Enhance Driving Scheme Capability
OLED_WR_Byte(0xa2);
OLED_WR_Byte(0x20);

OLED_WR_REG(0xbb);     //Set Pre-Charge Voltage
OLED_WR_Byte(0x1f);

OLED_WR_REG(0xb6);     //Set Second Pre-Charge Period
OLED_WR_Byte(0x08);

OLED_WR_REG(0xbe);     //Set VCOMH Deselect Level
OLED_WR_Byte(0x07);

OLED_WR_REG(0xa6);     //Set Display Mode
```

```
      OLED_WR_REG 0xA9 ;    D sa   e Part a  D sp ay
      OLED_Fill(0,0,256,64,0x00);      //Clear Screen

      OLED_WR_REG(0xaf);      //Sleep Out}

#define OLED_CMD    0    //write command
#define OLED_DATA    1    //write data

void OLED_WR_Byte(u8 dat,u8 cmd)
{
    u8 i;
    if(cmd)
       OLED_DC_Set();
    else
       OLED_DC_Clr();
    OLED_CS_Clr();
    for(i=0;i<8;i++)
    {
     OLED_SCL_Clr();
     if(dat&0x80)
          OLED_SDA_Set();
     else
          OLED_SDA_Clr();
     OLED_SCL_Set();
     dat<<=1;
    }
    OLED_CS_Set();
    OLED_DC_Set();
}
```