SURENOO GRAPHIC OLED SERIES DISPLAY

Product Specification

Part Name: OEL Display Module

SOG25664B2_M312

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Graphic OLED Display Selection Guide

Graphic OLED Module | **Graphic OLED Panel**

SSD1362

Contents

1. Basic Specifications

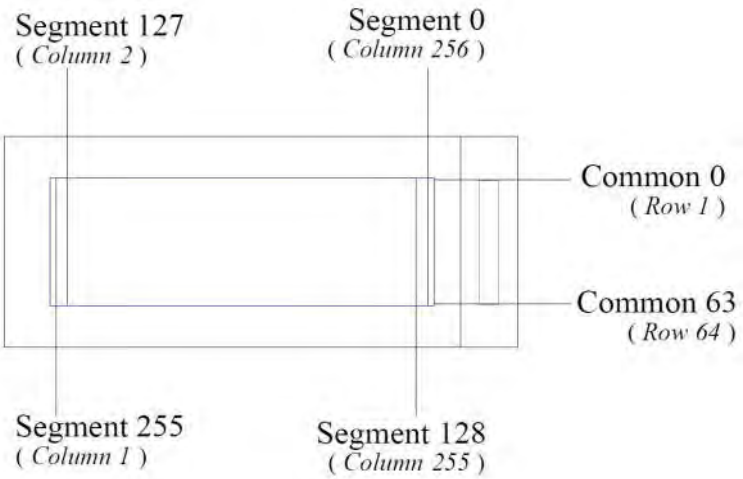
1.1 Display Specifications

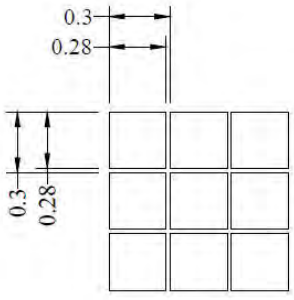
1) Display Mode : Passive Matrix
2) Display Color : Monochrome with 16 Gray Scales (White)
3) Drive Duty : 1/64 Duty

1.2 Mechanical Specifications

1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 256 × 64
3) Module Size : 100.0× 33.0 × 5.4 (mm) -16P
   100.0× 30.0 × 5.4 (mm) -7P
   100.0× 30.0 × 5.4 (mm) -5P
4) Panel Size : 86.9 × 25.8 × 2.0 (mm) including "Anti-Glare Polarizer"
5) Active Area : 76.78 × 19.18 (mm)
6) Pixel Pitch : 0.3 × 0.3 (mm)
7) Pixel Size : 0.28 × 0.28 (mm)
8) Weight : TBD (g) ± 10%

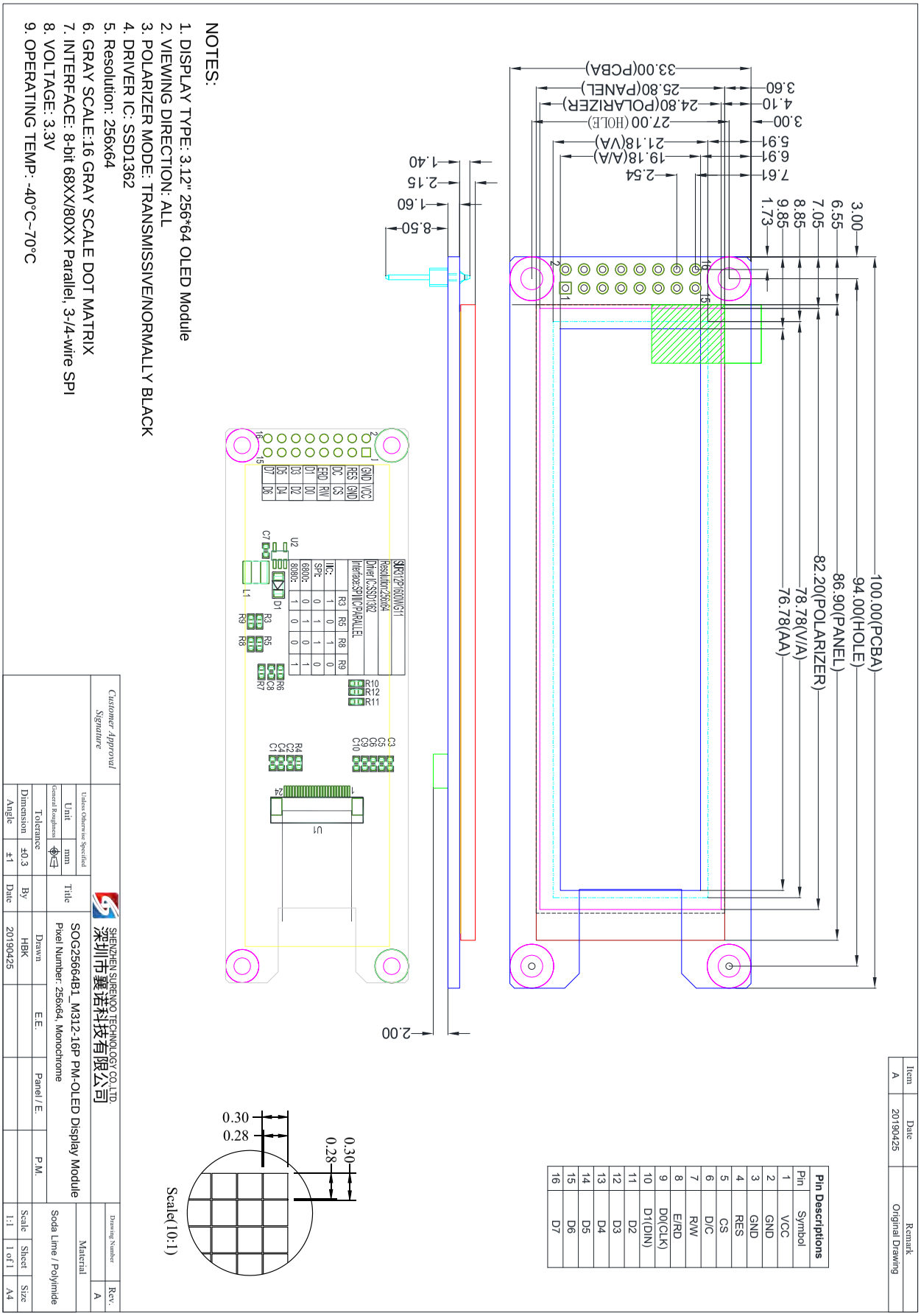
1.3 Active Area / Memory Mapping & Pixel Construction





Pixel Detail
Scale (10:1)

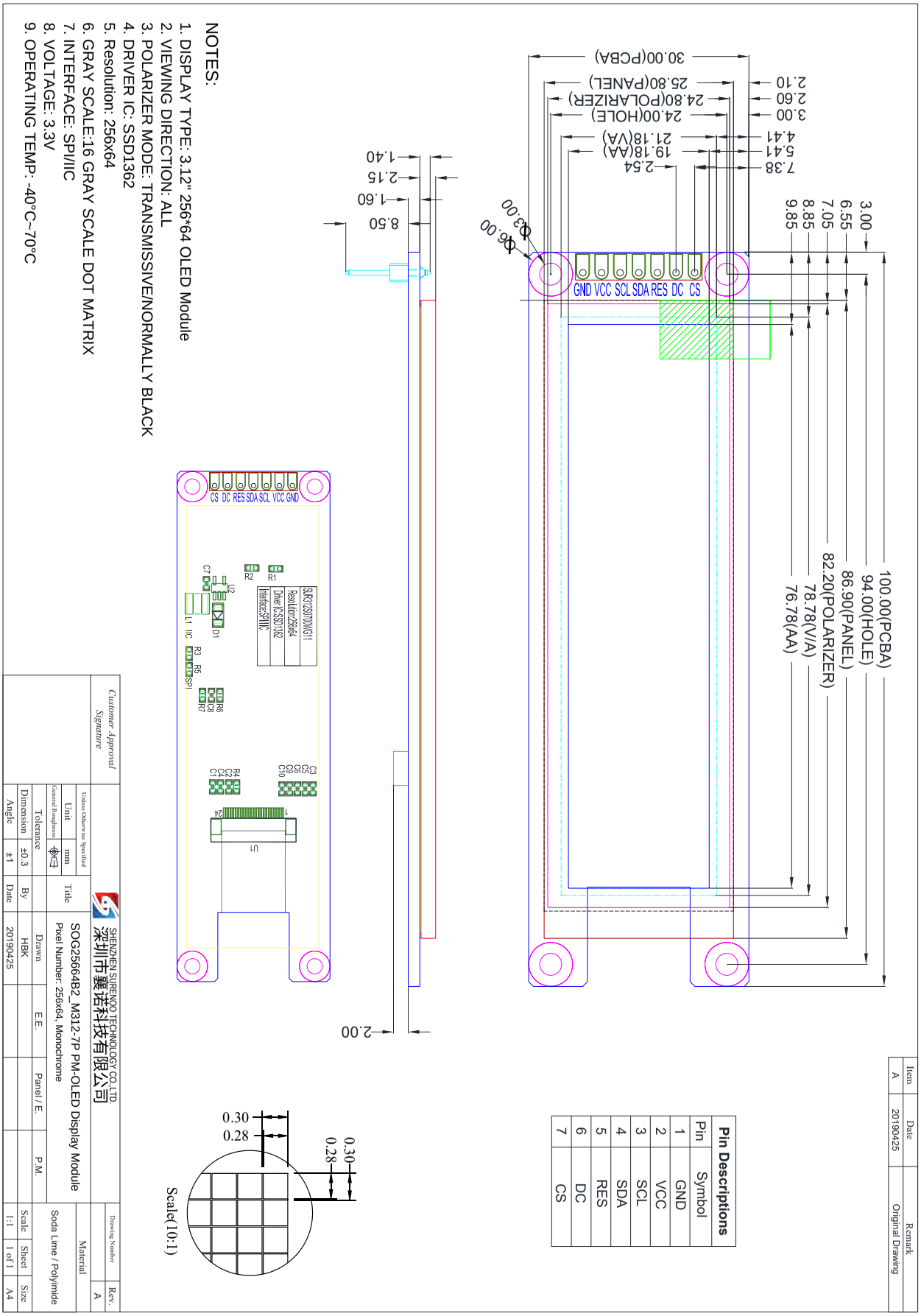
3. EXTERNAL DIMENSIONS



1.5.1 Pin Definition (SOG25664B2-M312-16P)

PIN No.	Symbol	Description
1	VCC	Power Supply for OLED This is a voltage supply pin. It must be connected to source
2	GND	Ground of Logic Circuit This is a ground pin. It must be connected to ground
3	GND	Ground of Logic Circuit This is a ground pin. It must be connected to ground
4	RES	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation
5	CS	Chip Select This pin is the chip select pin. Low enable, high disable.
6	DC	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at SDA is treated as display data. When the pin is pulled low, the input at SDA will be transferred to the command register.
7	R/S	Serves as a read signal and MCU read data at the rising edge.
8	E/RD	Serves as a write signal and MCU write data at the rising edge.
9-16	D0-D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.

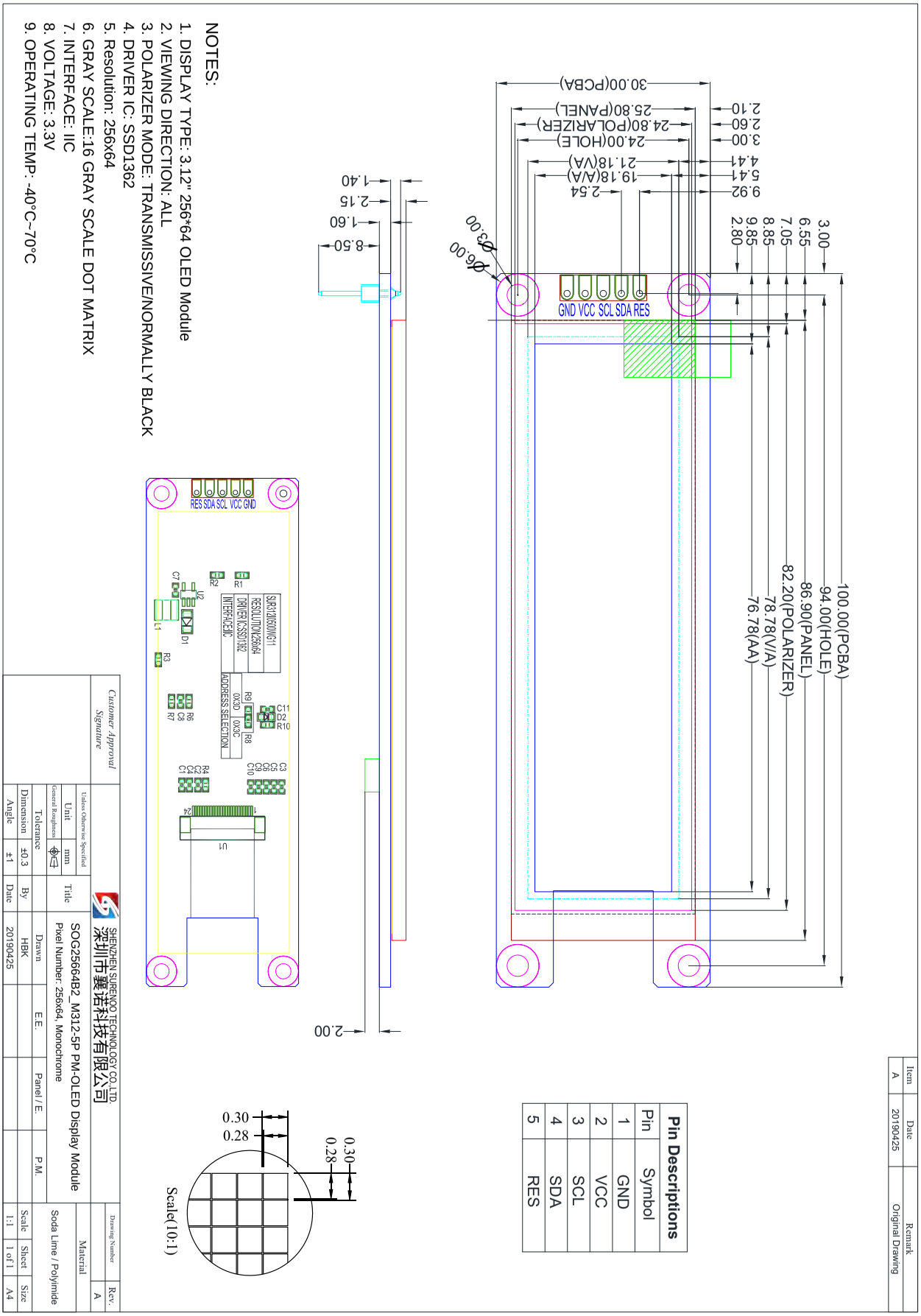
3. EXTERNAL DIMENSIONS



1.5.2 Pin Definition (SOG25664B2-M312-7P)

Pin Number	Symbol	I/O	Function
Power Supply			
1	GND	P	**Ground** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
2	VCC	P	**Power Supply for Core and I/O** This is a voltage supply pin. It must be connected to external source 3.3V.
Interface			
3	SCL	I	**Host Data Input/Output Bus** When SPI mode is selected, SCL is the serial clock input, SPI CLK. When I2C mode is selected, SCL is the serial clock input, I2C SCL.
4	SDA	I	**Host Data Input/Output Bus** When SPI mode is selected, SDA is the serial data input, SPI DATA(MOSI). When I2C mode is selected, SDA is the serial data input, I2C SDA.
5	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
6	D/C#	I	**Data/Command Control** When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register.
7	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

3. EXTERNAL DIMENSIONS



1.5.3 Pin Definition (SOG25664B2-M312-5P)

Pin Number	Symbol	I/O	Function
Power Supply			
1	GND	P	**Ground** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
2	VCC	P	**Power Supply for Core and I/O** This is a voltage supply pin. It must be connected to external source 3.3V.
Interface			
3	SCL	I	**Host Data Input/Output Bus** When SPI mode is selected, SCL is the serial clock input, SPI CLK. When I2C mode is selected, SCL is the serial clock input, I2C SCL.
4	SDA	I	**Host Data Input/Output Bus** When SPI mode is selected, SDA is the serial data input, SPI DATA(MOSI). When I2C mode is selected, SDA is the serial data input, I2C SDA.
5	RES	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	3	3.5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (100 cd/m^2)		TBD	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 7	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.29	0.29 0.33	0.33 0.37	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

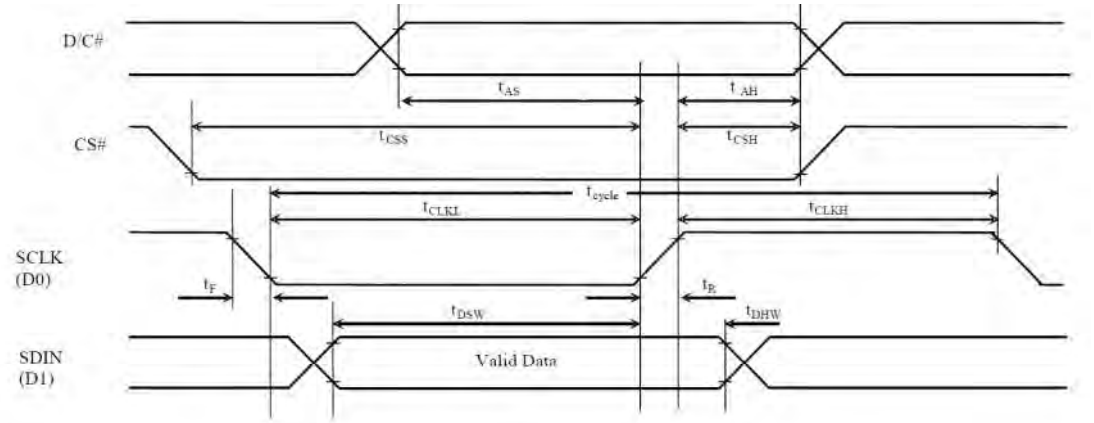
* Optical measurement taken at V_{DDIO} = 3.0V, V_{CC} = 12.0V.
Software configuration follows Section 4.5 Initialization.

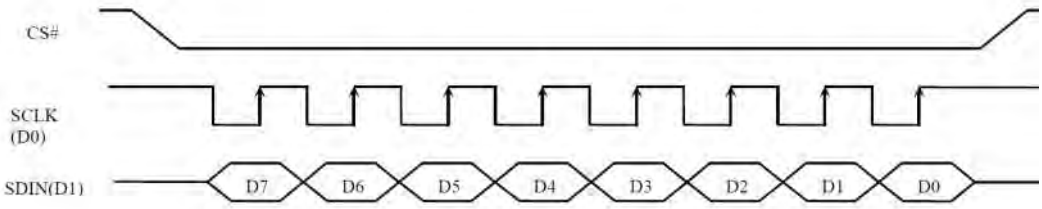
3.2 AC Characteristics

Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	40	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	30	-	ns
t_{CLKL}	Clock Low Time	25	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.5V, T_a = 25°C)





3.3 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

- Slave address bit (SA0)
  SSD1362 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

  b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
  0 1 1 1 1 0 SA0 R/W#

  "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1362. D/C# pin acts as SA0 for slave address selection. "R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

- I²C-bus data signal (SDA)
  SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

  It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

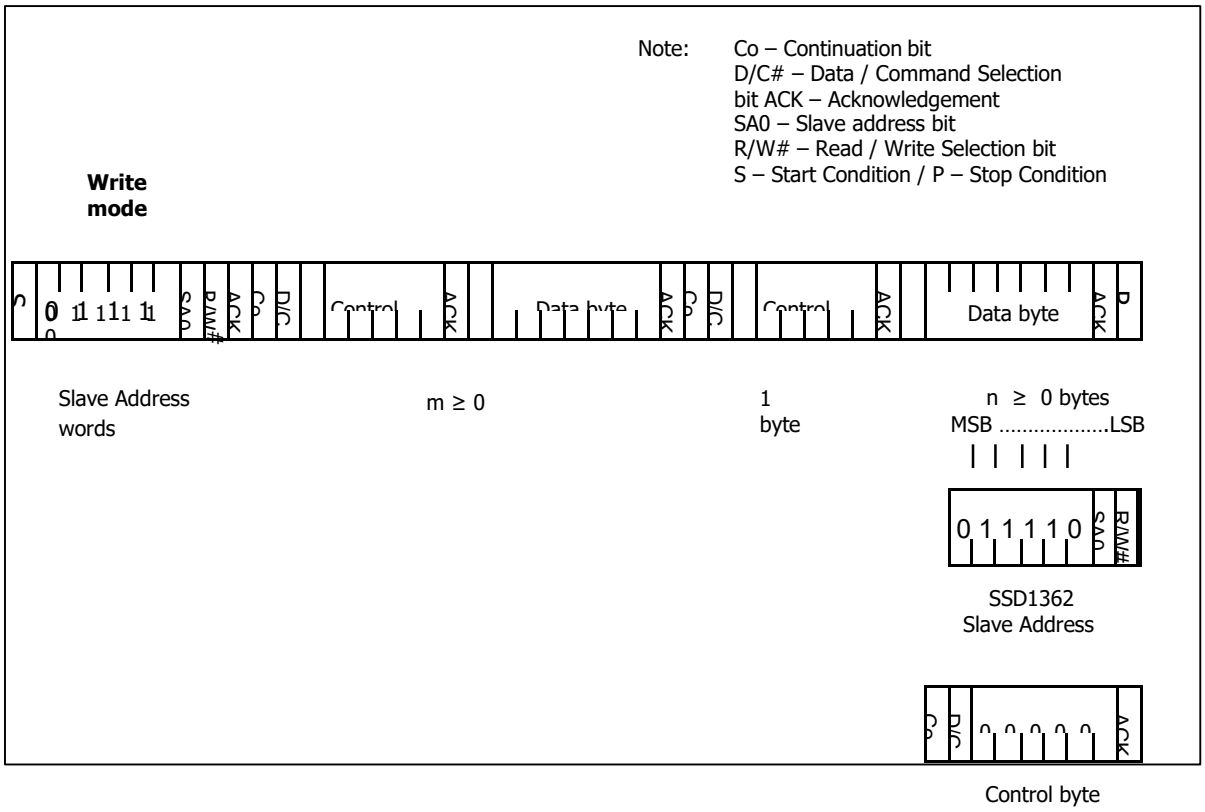
  "SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

- I²C-bus clock signal (SCL)
  The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

3.3 I2C-bus Write data

The I^2C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I^2C-bus in chronological order.

Figure 7-7 : I2C-bus data format



- Write mode for I^2C
  - The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
  - The slave address is following the start condition for recognition use. For the SSD1362, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
  - The write mode is established by setting the R/W# bit to logic "0".
  - An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
  - After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"'s.
    - If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    - The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically

after each data write.

- Acknowledge bit will be generated after receiving each control byte or data byte.
- The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure : Definition of the Start and Stop Condition

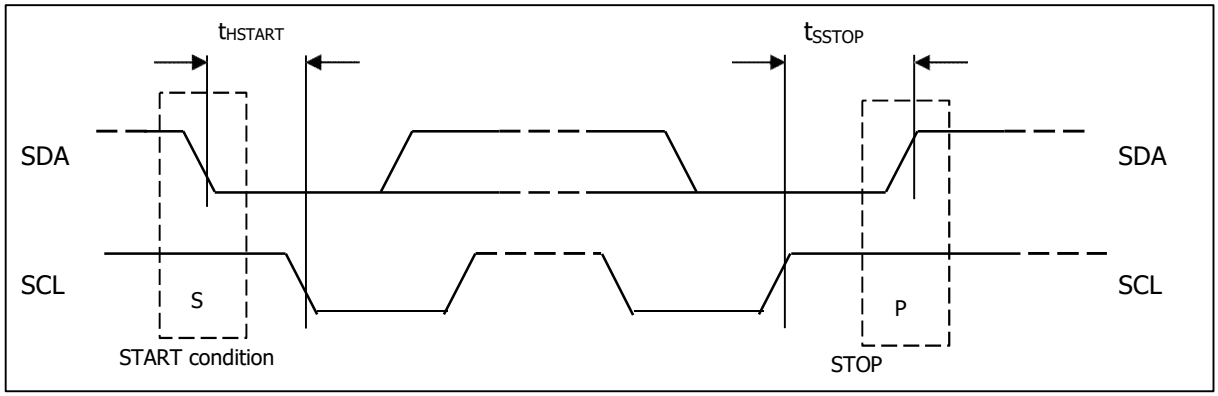
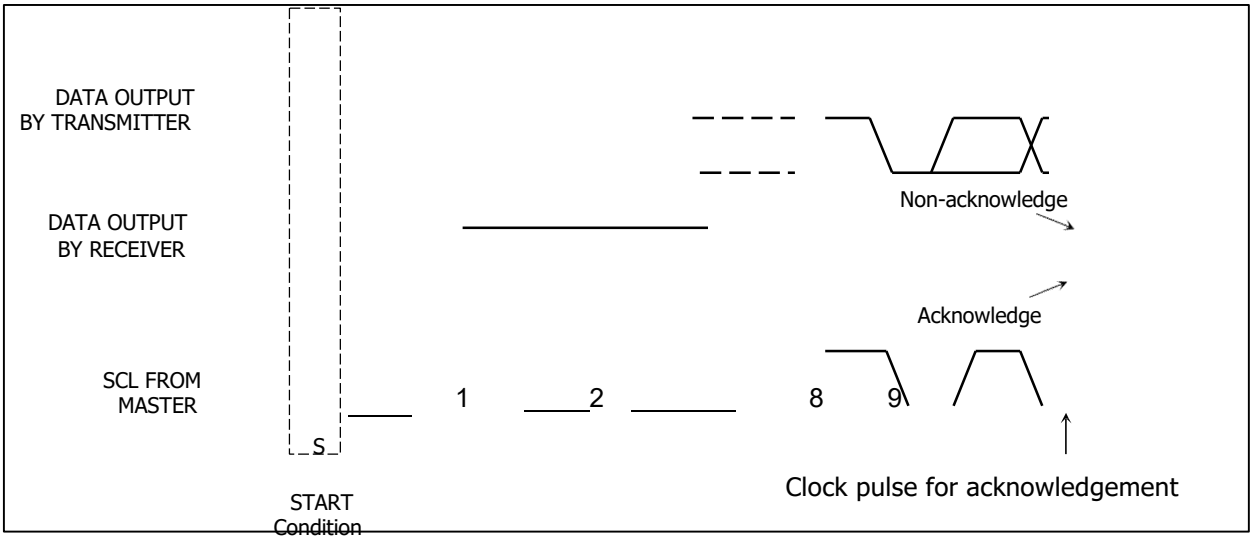


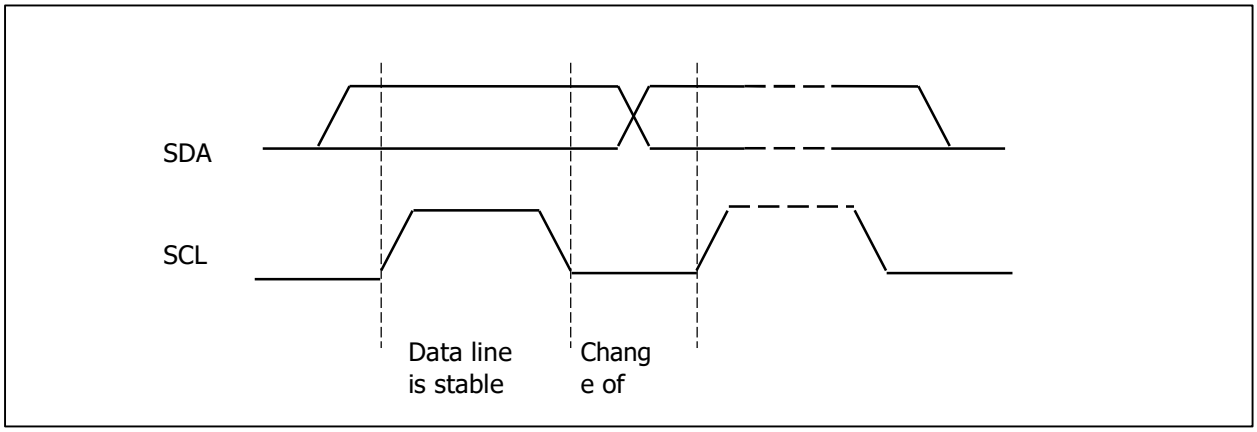
Figure 7-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

2. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
3. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition

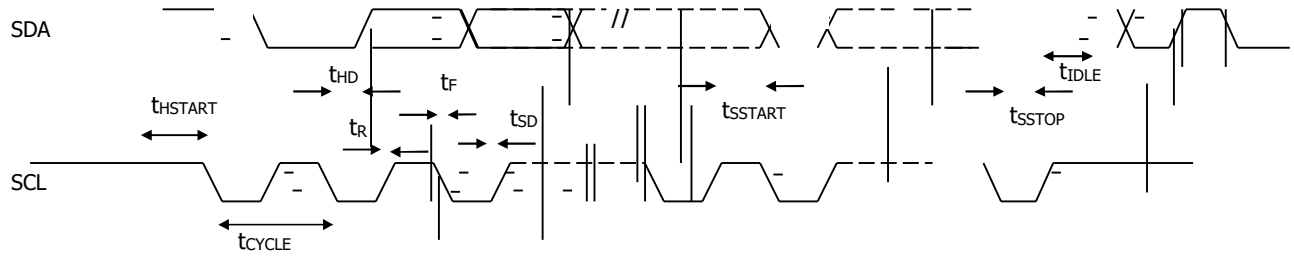


- **I2C Timing Characteristics**

(V_{CI} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Uni
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 12-5: I2C interface Timing



MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write. A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

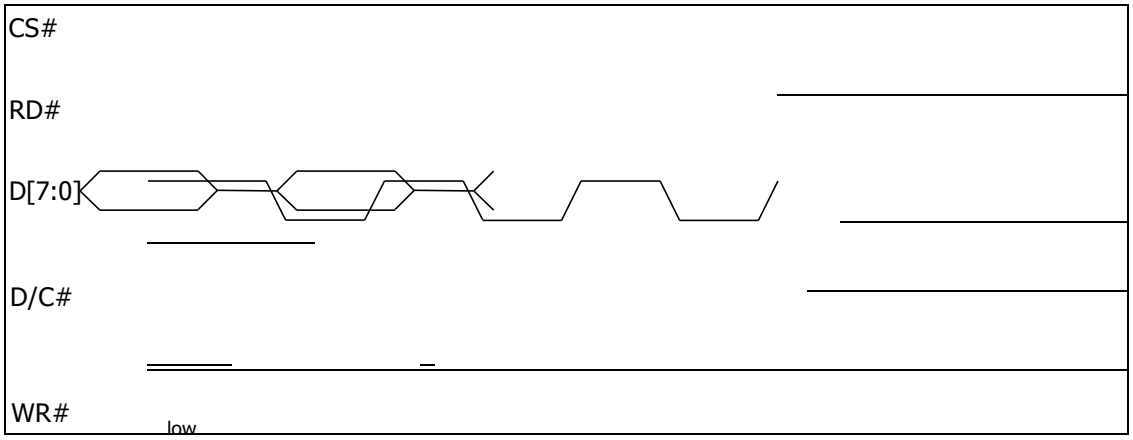


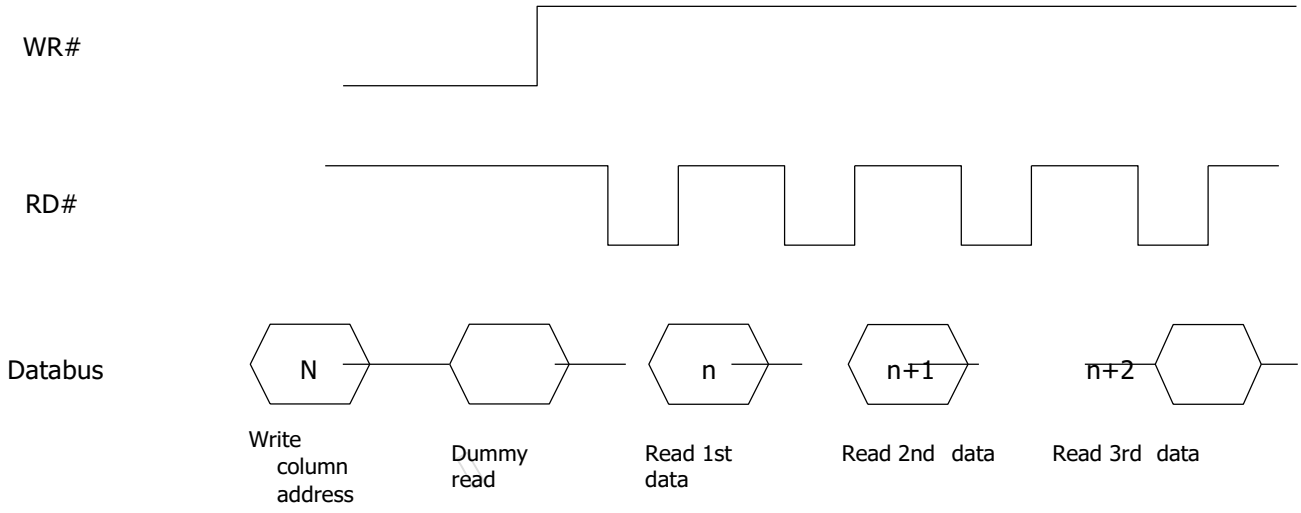
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



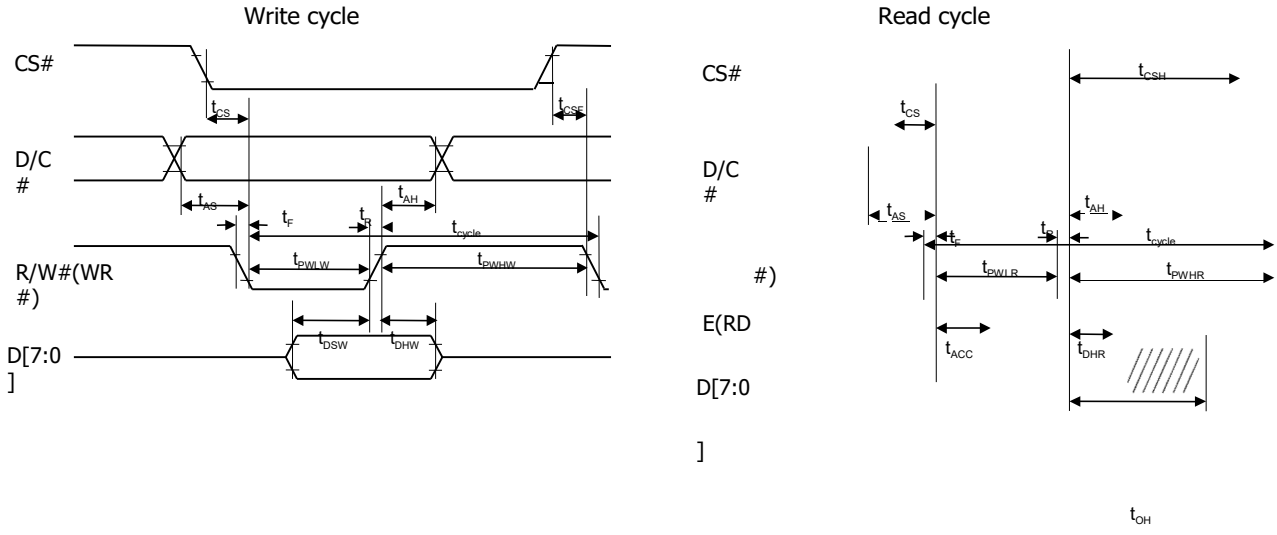
- 8080-Series MCU Parallel Interface Timing Characteristics

Table: 8080-Series MCU Parallel Interface Timing Characteristics

V_{CI} - V_{SS} = 1.65V to 3.5V (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Uni
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure : 8080-series MCU parallel interface characteristics



4. Functional Specification

4.1 Commands

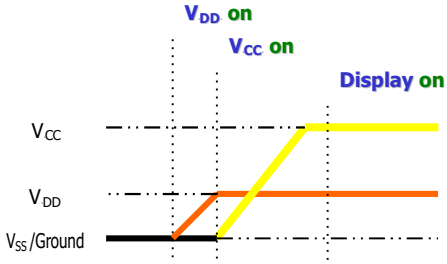
Refer to the Technical Manual for the SSD1362

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

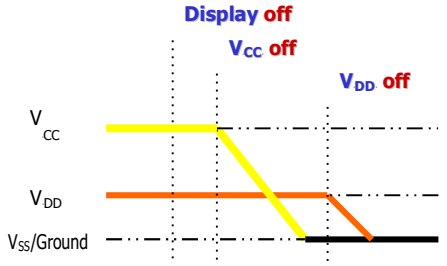
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 8:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

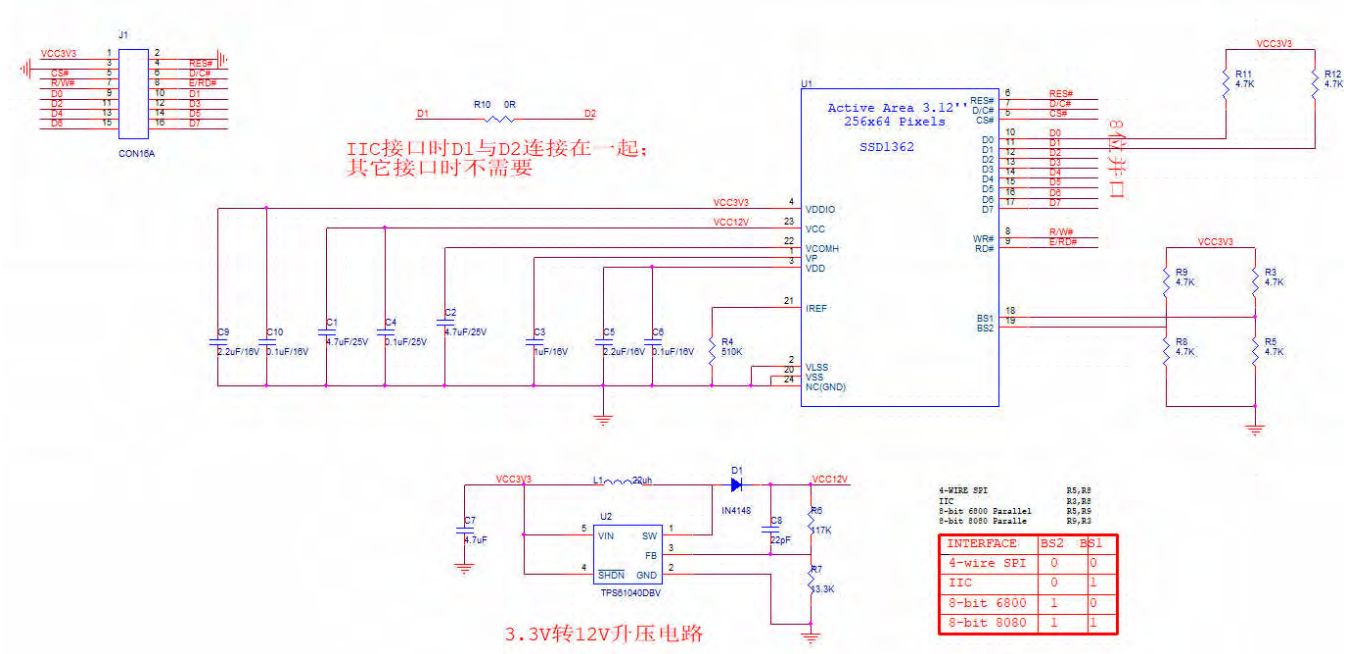
4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

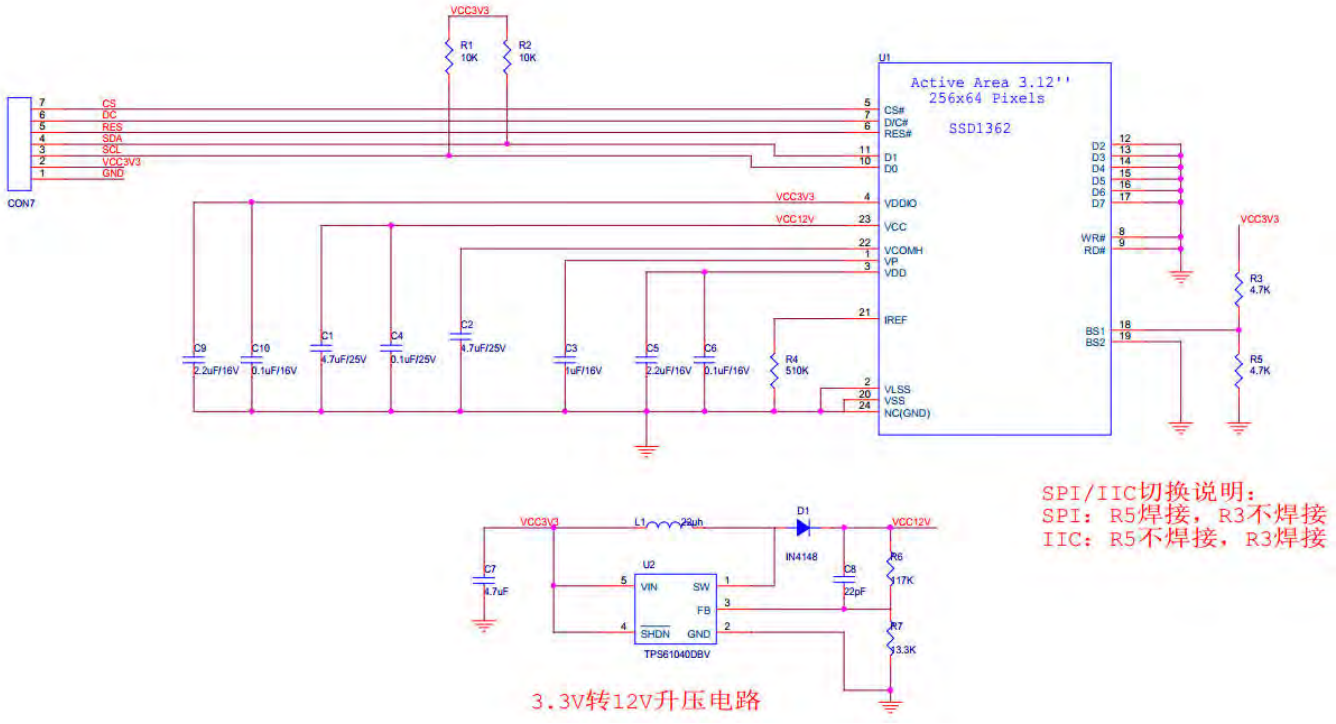
2. Display is OFF
3. 256×64 Display Mode
4. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
5. Shift register data clear in serial interface
6. Display start line is set at display RAM address 0
7. Column address counter is set at 0
8. Normal scan direction of the COM outputs
9. Contrast control register is set at 7Fh
10. Normal display mode (Equivalent to A4h command)

4.4 Application Circuit (VCC>3V)

4.4.1 SOG25664B2-M312-16P Interface

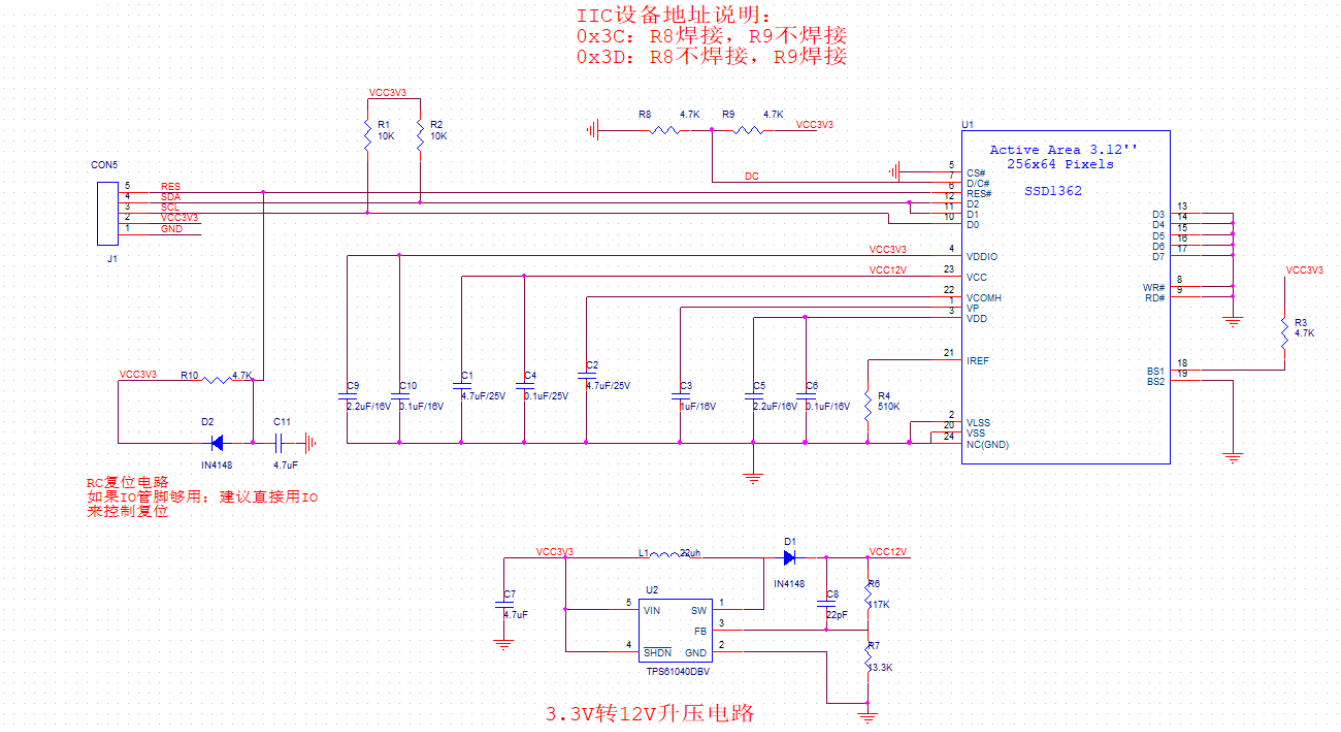


4.4.2 SOG25664B2-M312-7P Interface



默认为SPI接口；如果需要用IIC接口；需要讲电阻R5拆下来换到R3位置；同时CS,DC管脚接地。此时MCU与SCL；SDA及RES管脚连接；RES需要连接MCU管脚；不能直接接电源，请注意。

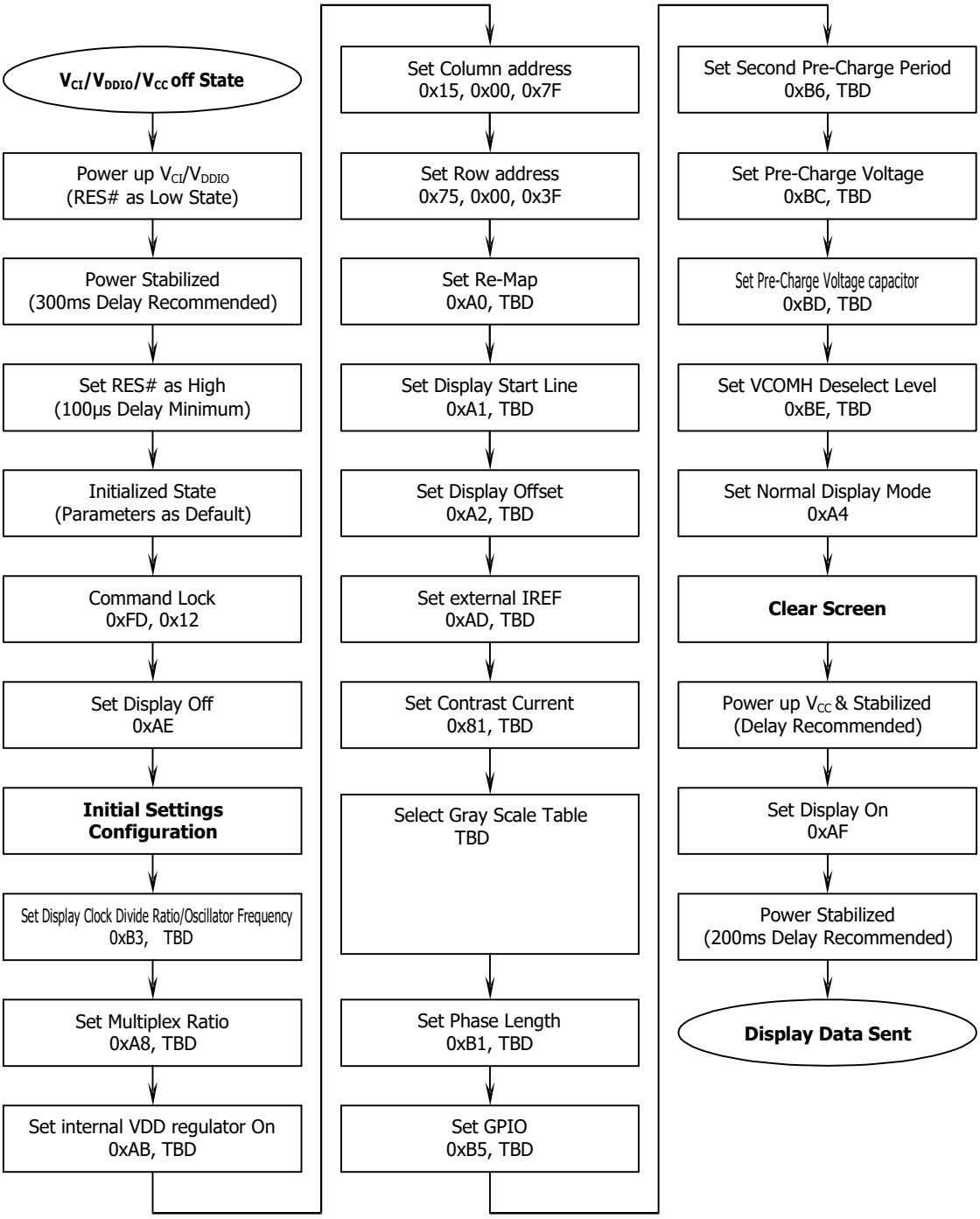
4.4.3 SOG25664B2-M312-5P Interface



4.5 Actual Application Example

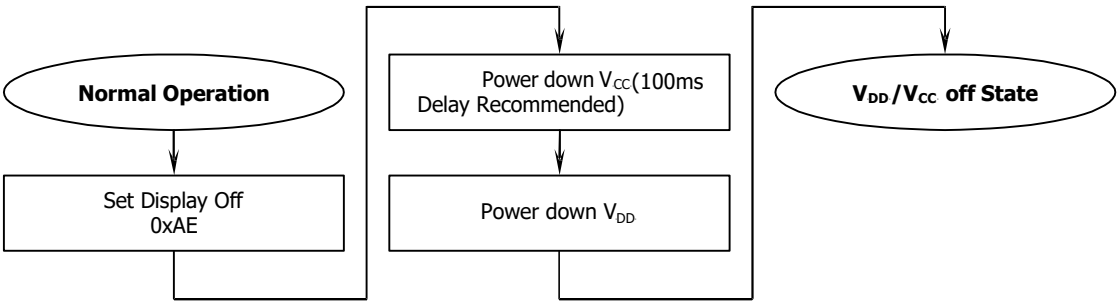
Command usage and explanation of an actual example (VDDIO>2.6V)

<Power up Sequence>

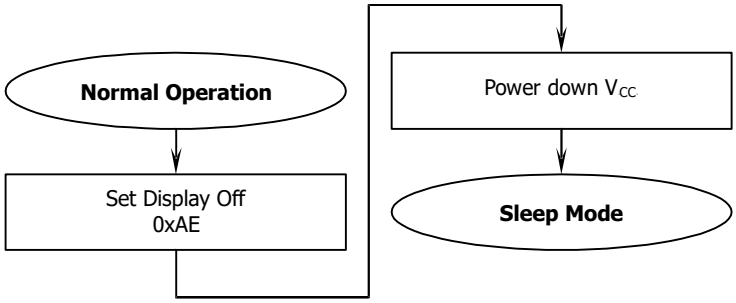


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

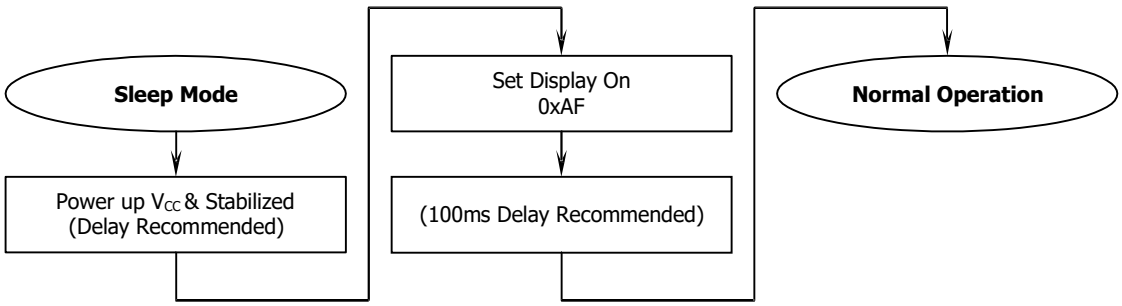
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

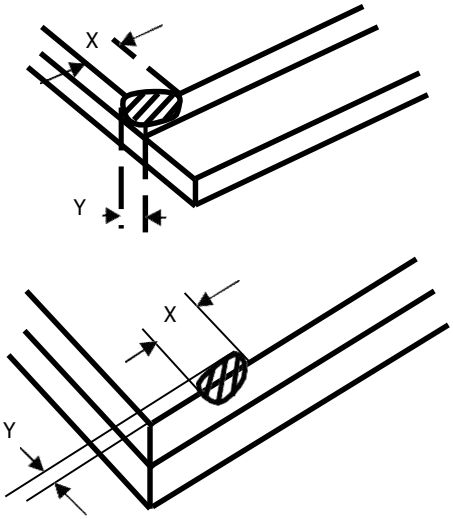
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

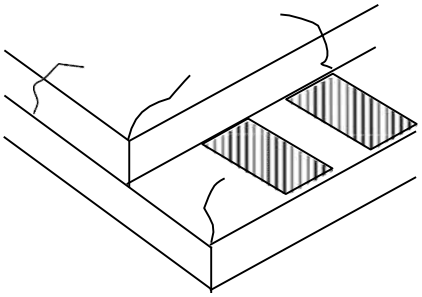
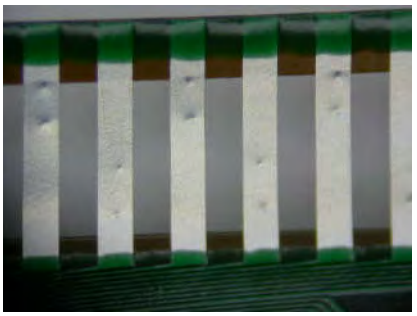
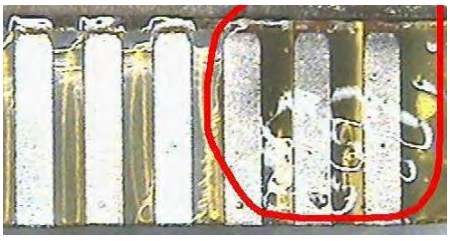
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

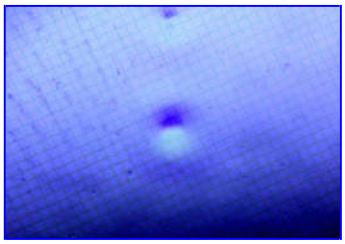
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

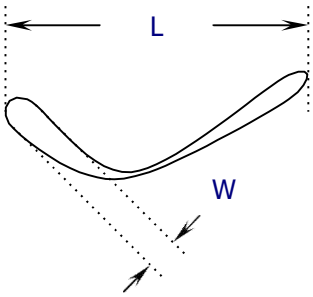
6.3.2 Cosmetic Check (Display Off) in Active Area

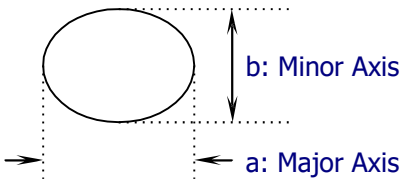
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for not Affect the Panel
Scratches, Fiber, Line-Shape Defect (On Display)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Display)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Display)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Panel)	Minor	Not Allowable

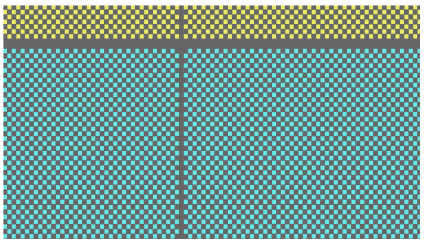
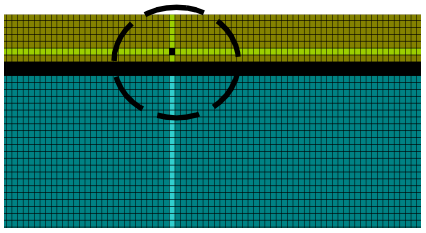
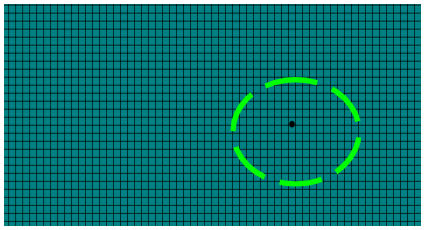
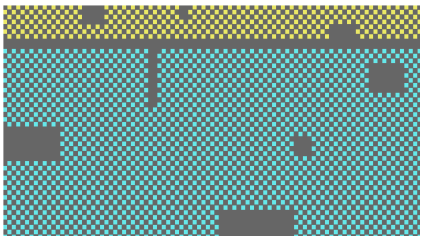
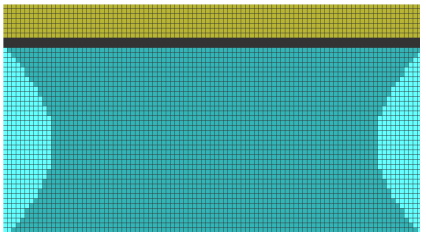
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2

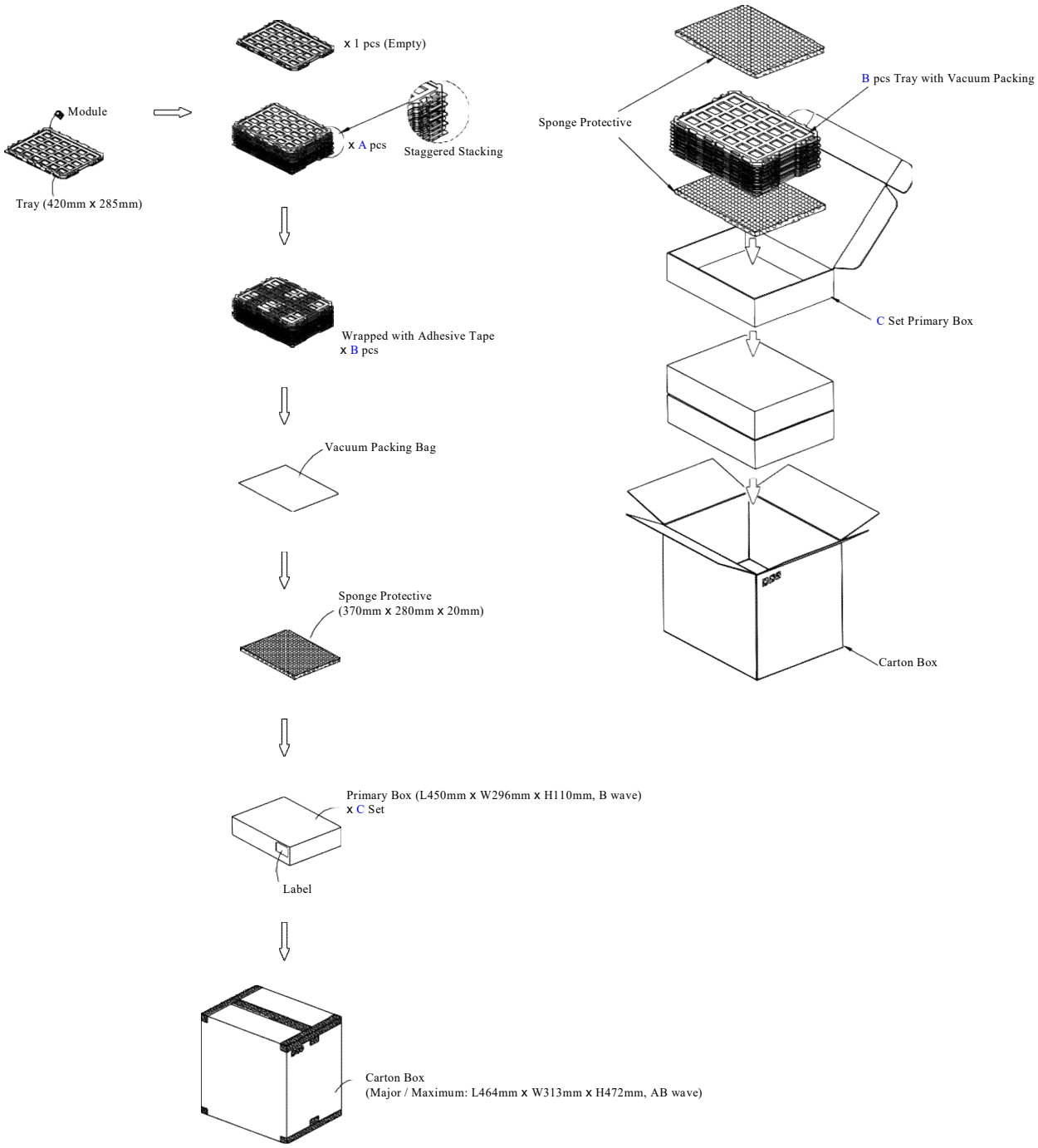




6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



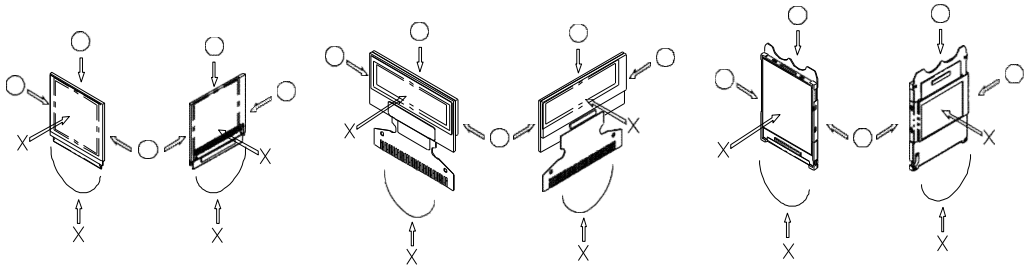
Item		Quantity	
Module		**TBD**	**per Primary Box**
Holding Trays	**(A)**	**TBD**	**per Primary Box**
Total Trays	**(B)**	**TBD**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Even the display is being made of plastic, do not apply mechanical impacts such us dropping or striking the module.
2) If the display is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The substrate of the OEL display module is soft but easily crack. Please be careful when handling the OEL display module.
5) When the surface of the substrate of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the substrate will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the substrate:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the display and FPC tails with electrode pattern layouts. These stresses will influence the display performance.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high

humidity environment or low temperature (less than 0 C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Zhengzhou Zhongjingyuan Electronic Technology Co., LTD.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about theabove.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1307
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation

statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. Zhengzhou Zhongjingyuan Electronic Technology Co., LTD. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

Notice: