SURENOO GRAPHIC OLED SERIES DISPLAY

Product Specification

Part Name: OEL Display Module

SOG12864A_M270

Please click the following image to buy the sample

Shenzhen Surenoo Technology Co.,Ltd.
www.surenoo.com
E-mail: info@surenoo.com

Graphic OLED Display Selection Guide

Graphic OLED Module | **Graphic OLED Panel**

SSD1325

1. FUNCTIONS & FEATURES

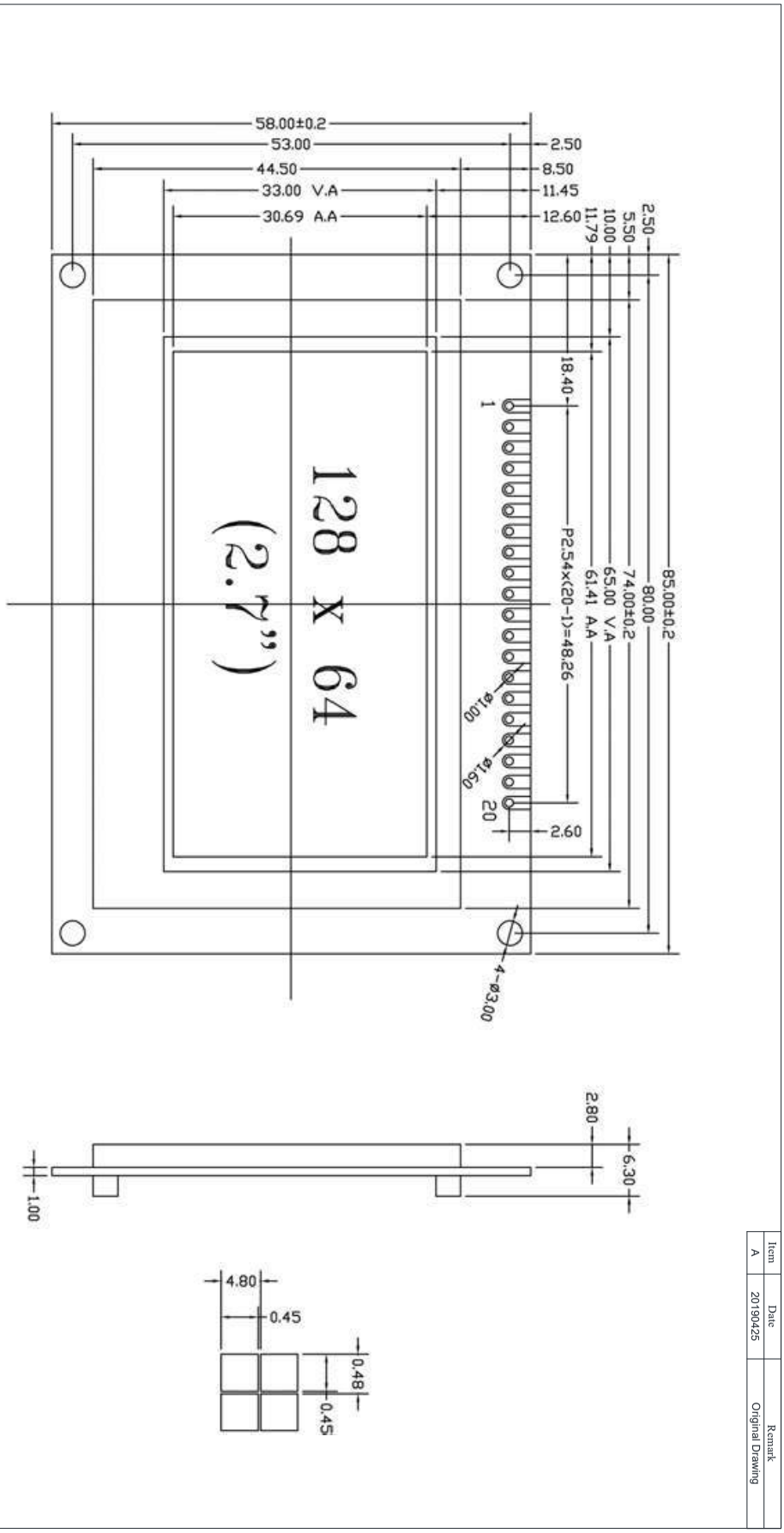
Features

- 128X64 dots
- Font Color: YELLOW/WHITE/GREEN
- Driver IC:SSD1325
- 8-BIT 68XX/80XX Parallel, SPI

2. MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	85.0L×58.0W×6.3H	mm
View Area	65.0×33.0	mm
Effective Area	128×64	dots
Pixel Size	0.45×0.45	mm
Pixel Pitch	0.48×0.48	mm

3. EXTERNAL DIMENSIONS



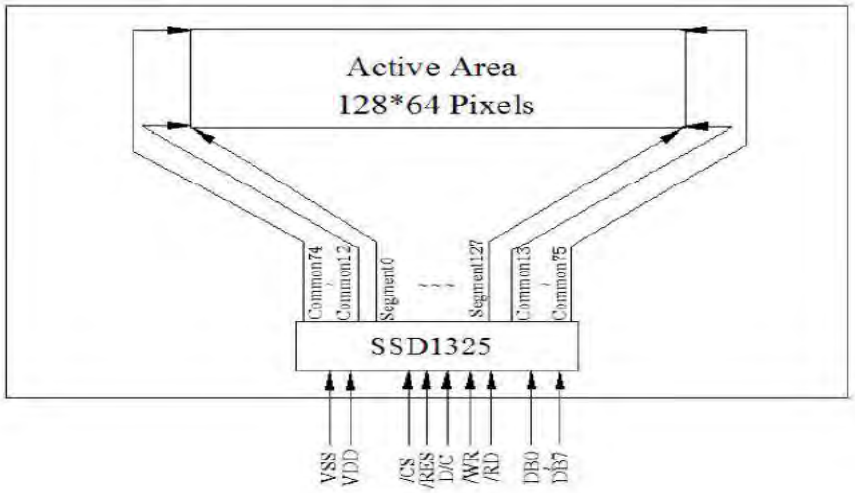
NOTES:

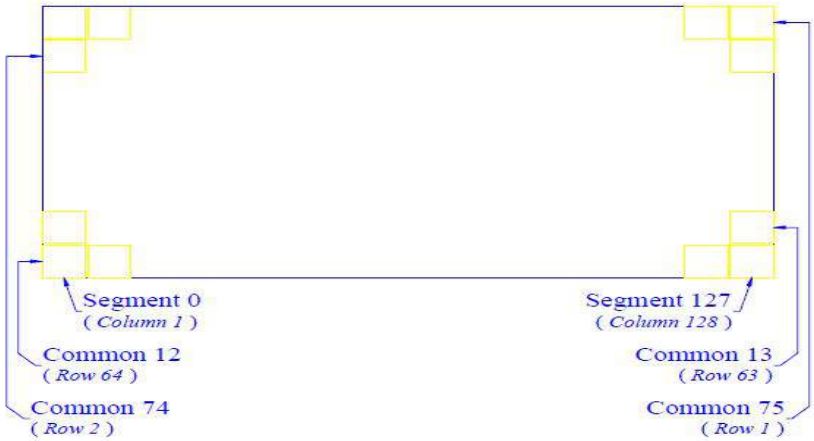
1. DISPLAY TYPE: 2.7" 128*64 OLED
2. VIEWING DIRECTION: ALL
3. POLARIZER MODE: TRANSMISSIVE/NORMALLY BLACK
4. DRIVER IC: SSD1325
5. Resolution: 128x64
6. INTERFACE: 8-bit 68XX/80XX Parallel, 3-/4-wire SPI
7. VOLTAGE: 3.3V
8. OPERATING TEMP: -40°C~70°C

Item	Date	Remark
A	20190425	Original Drawing

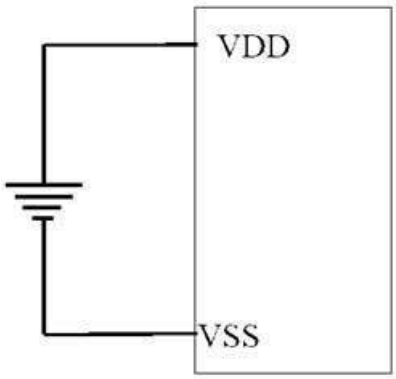
Customer Approval Signature						
	Unless Otherwise Specified		SHENZHEN SURENOO TECHNOLOGY CO.,LTD. 深圳市襄诺科技有限公司			Rev.
	Unit	mm	Title		Drawing Number	A
	General Roughness		SOG12864A_M270 PM-OLED Display Module Pixel Number: 128x64, Monochrome		Material	
	Tolerance		Drawn	E.E.	Panel / E.	P.M.	Soda Lime / Polyimide	
	Dimension	±0.3	HBK				Scale	Sheet	Size
	Angle	±1	By				1:1	1 of 1	A4
			Date	20190425					

4. BLOCK DIAGRAM





5. POWER SUPPLY



6. PIN DESCRIPTION

Parallel Interface(8080): (R18,R20 USE; R19,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	VSS	0V	Power Ground
2	VBAT	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data L：Command
5	WR	H/L	8080:Active LOW Write signal
6	RD	H/L	8080: Active LOW Read signal
7~14	D0～D7	H/L	Data Bus
15	/CS	L	Chip Select
16	/RST	H/L	Active LOW Reset signal
17~19	NC	—	No connection
20	FG	0V	Power Ground

Parallel Interface(6800): (R19,R20 USE; R18,R21 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	VSS	0V	Power Ground
2	VBAT	+3.3~+5.0V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data L：Command
5	WR	H/L	6800:Read/Write select signal, R/W=1: Read R/W: =0: Write
6	RD	H/L	6800:Operation enable signal. Falling edge triggered.
7~14	D0～D7	H/L	Data Bus
15	/CS	L	Chip Select
16	/RST	H/L	Active LOW Reset signal
17~19	NC	—	No connection
20	FG	0V	Power Ground

SPI: (R19,R21 USE; R18,R20 NO USE)

ITEM	SYMBOL	LEVEL	FUNCTION
1	VSS	0V	Power Ground
2	VBAT	+3.3~+ 5.0V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data L：Command
5	WR	0V	Power Ground
6	RD	0V	Power Ground
7	SCLK(D0)	H/L	Serial Clock signal
8	SDIN(D1)	H/L	Serial Data input signal
9	DB2	-	No connect
10~14	DB3～DB7	0V	Power Ground
15	/CS	L	Chip Select
16	/RST	H/L	Active LOW Reset signal
17~19	NC	—	No connection
20	FG	0V	Power Ground

Table 6 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

7． AbsoluteMaximumRatings

Parameter	Symbol	Min	Max	Unit	Notes
Power Supply	VBAT	3.3	5	V	-
Logic Supply Voltage	VDD	2.5	3.3	V	1, 2
Supply Voltage for Display	Vcc	0	15	V	1, 2
Supply Current	Ivbat	-	110	mA	1, 2
Operating Temperature	Top	-40	85	℃	-
Storage Temperature	Tst	-45	90	℃	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

8 . ELECTRICAL CHARACTERISTICS

8.1 DC Charateristics

Items	Symbol	Condition	Min	TYP	Max	Unit
Operating Temperature Range	Top	Absolute Max	-40	—	+85	℃
Storage Temperature Range	Tst	Absolute Max	-45	—	+90	℃
Supply Voltage	VDD		2.8	3.0	3.3	V
High Level input	VIH	Iout=100Ua,3.3MHz	0.8*VDD	—	VDD	V
Low Level input	VIL	Iout=100Ua,3.3MHz	0	—	0.2*VDD	V
Supply Current (logic)	IDD	Note	—	8	—	mA
Display voltage	VCC	Ta=25℃	14.5	15	15.5	V

Note:VDD=3.3V,VCC=12.5V(VDD,VCC Supply by the module internal generate) 100% Display Area Turn on.

9 . Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		—	80	—	
Viewing Angle – Bottom	AV		—	80	—	
Viewing Angle – Left	AH		—	80	—	
Viewing Angle – Right	AH		—	80	—	
Contrast Ratio	Cr		2000:1	—	—	—
Response Time (rise)	Tr	—	—	10	—	us
Response Time (fall)	Tf	—	—	10	—	us
Brightness		50% checkerboard	100	120	—	cd/m2
Lifetime		Ta=25°C, 50% checkerboard	10,000	—	—	Hrs

Note: Lifetime at typical temperature is based on accelerated high‐temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until Half‐Brightness. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn‐in) images may occur. To avoid this, every pixel should be illuminated uniformly.

10. COMMAND TABLE

Built - in SSD1325 controller.

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	15	0	0	0	1	0	1	0	1	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00h
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0	75	0	1	1	1	0	1	0	1	Set Row address	Second command A[6:0]sets the row start address from 0-79, RESET = 00h
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		Third command B[6:0] sets the row end address from 0-79, RESET = 4Fh
0	81	1	0	0	0	0	0	0	1	Set Contrast Current	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		The level is set to 40h after RESET
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84h = Quarter Current Range (RESET) 85h = Half Current Range 86h = Full Current Range
0	A0	1	0	1	0	0	0	0	0	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (RESET) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (RESET) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (RESET) A[4]=1, Enable COM Re-map A[5]=0, Reserved (RESET) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (RESET) A[6]=1, Enable COM Split Odd Even
0	A1	1	0	1	0	0	0	0	1	Set Display Start Line	Set display RAM display start line register from 0-79 Display start line register is reset to 00h after RESET
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by COM from 0-79 The value is reset to 00H after RESET
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Normal Display (RESET) A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Entire Display OFF, all pixels turns OFF A7h = Inverse Display
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 1	1 A_0	Set Master Configuration	A[0] = 0, Select external V_{CC} supply A[0] = 1, Reserved (RESET) **Note** (1) Bit A[0] **must be** set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display OFF	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display ON	AFh = Display ON
0 0	B0 A[5:0]	1 *	0 *	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET) A[5:0] = 28h, Enable pre-charge compensation
0 0 0	B1 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	0 A_1 *	1 A_0 *	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h Note (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Row Period (set frame frequency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	B3	1	0	1	1	0	0	1	1	Set Display Clock Divide Ratio / Oscillator Frequency	The lower nibble (A[3:0]) of the next command defines the divide ratio (D) of display clock (DCLK) Divide ratio (D)=A[3:0]+1 (A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2) The higher nibble (A[7:4]) of the next command sets the Oscillator Frequency Oscillator Frequency increases with the value of A[7:4] and vice versa Range: 0000b~1111b RESET= 0100b represents 630KHz, typical step value: 5% of previous value
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	A[7:4]	A_7	A_6	A_5	A_4	*	*	*	*		
0	B4	1	0	1	1	0	1	0	0	Set Pre-charge	A[2:0] = 0 (RESET)
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0	Compensation Level	A[2:0] = 3h, Recommended level
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below: A[2:0] = Gray scale level of GS1, RESET=1 B[2:0] = Gray scale level of GS2, RESET=1 B[6:4] = Gray scale level of GS3, RESET=1 C[2:0] = Gray scale level of GS4 RESET=1 C[6:4] = Gray scale level of GS5, RESET=1 D[2:0] = Gray scale level of GS6, RESET=1 D[6:4] = Gray scale level of GS7, RESET=1 E[2:0] = Gray scale level of GS8, RESET=1 E[6:4] = Gray scale level of GS9, RESET=1 F[2:0] = Gray scale level of GS10, RESET=1 F[6:4] = Gray scale level of GS11, RESET=1 G[2:0] = Gray scale level of GS12, RESET=1 G[6:4] = Gray scale level of GS13, RESET=1 H[2:0] = Gray scale level of GS14, RESET=1 H[6:4] = Gray scale level of GS15, RESET=1
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	B[6:4]	*	B_6	B_5	B_4	*	*	*	*		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	C[6:4]	*	C_6	C_5	C_4	*	*	*	*		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	D[6:4]	*	D_6	D_5	D_4	*	*	*	*		
0	E[2:0]	*	*	*	*	*	E_2	E_1	E_0		
0	E[6:4]	*	E_6	E_5	E_4	*	*	*	*		
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		
0	F[6:4]	*	F_6	F_5	F_4	*	*	*	*		
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		
0	G[6:4]	*	G_6	G_5	G_4	*	*	*	*		
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		
0	H[6:4]	*	H_6	H_5	H_4	*	*	*	*		
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level, A[7:0] 1xxxxxxx connects to V_{COMH} 001xxxxx 1.0 * V_{REF} 00000000 0.51* V_{REF} 00000001 0.52* V_{REF} ..... 00011000 0.75* V_{REF} (RESET) ..... 00011111 0.84* V_{REF}
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Second command A[4:0] sets the V_{COMH} voltage level , A[4:0] 00000 0.51*V_{REF} 00001 0.52* V_{REF} ..... 10001 0.68* V_{REF} (RESET) ..... 11101 0.81* V_{REF} 11110 0.82* V_{REF} 11111 0.84* V_{REF}
0	A[4 :0]	*	*	0	A4	A3	A2	A1	A0		

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	BF A[3:0]	1 *	0 *	1 *	1 *	1 A_3	1 A_2	1 A_1	1 A_0	Set Segment Low Voltage (VSL)	Second command A[3:0] sets the VSL voltage as follow: A[3:0] = 0010 kept VSL pin NC A[3:0] = 1110 (RESET) connect a capacitor between VSL pin and V_{SS}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Table 19: Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	23 A[4:0]	0 *	0 *	1 *	0 A_4	0 *	0 *	1 A_1	1 A_0	Graphic Acceleration Command Options	A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET) A[1] = 0b: Disable x-wrap(RESET) A[1] = 1b: Enable wrap around in x-direction during copying and scrolling A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0 0 0 0 0 0 0	24 A[5:0] B[6:0] C[5:0] D[6:0] E[7:0]	0 * * * * E_7	0 * B_6 * D_6 E_6	1 A_5 B_5 C_5 D_5 E_5	0 A_4 B_4 C_4 D_4 E_4	0 A_3 B_3 C_3 D_3 E_3	1 A_2 B_2 C_2 D_2 E_2	0 A_1 B_1 C_1 D_1 E_1	0 A_0 B_0 C_0 D_0 E_0	Draw Rectangle	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[7:0]: Set Gray scale pattern E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 31 for the gray scale pattern setting examples. **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$
0 0 0 0 0 0 0	25 A[5:0] B[6:0] C[5:0] D[6:0] E[5:0] F[6:0]	0 * * * * * *	0 * B_6 * D_6 * F_6	1 A_5 B_5 C_5 D_5 E_5 F_5	0 A_4 B_4 C_4 D_4 E_4 F_4	0 A_3 B_3 C_3 D_3 E_3 F_3	1 A_2 B_2 C_2 D_2 E_2 F_2	0 A_1 B_1 C_1 D_1 E_1 F_1	1 A_0 B_0 C_0 D_0 E_0 F_0	Copy	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
											E[5:0]: Column Address of New Start F[6:0]: Row Address of New Start **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$ (3) $0 \le E \le 63$ (4) $0 \le F \le 79$
0 0 0 0	26 A[5:0] B[6:0] C[1:0]	0 * * *	0 * B_6 *	1 A_5 B_5 *	0 A_4 B_4 *	0 A_3 B_3 *	1 A_2 B_2 *	1 A_1 B_1 C_1	0 A_0 B_0 C_0	Horizontal Scroll	A[5:0]: 1~63 horizontal offset in number of 2~127 column 0 no horizontal scroll B[6:0]: 2~80 number of rows to be H-scrolled C[1:0]: scrolling time interval 00b 12 frames 01b 64 frames 10b 128 frames 11b 256 frames **Note:** (1) Scrolling operates during display ON. (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Stop Moving	This command deactivates the scrolling action. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal Scroll command 26h. **Note** (1) The "wrap around in x-direction" function must be enabled before scrolling start. i.e. Bit A{1} of command 23h must be set to 1b before issuing 2F command.

Table 20: Read Command Table

(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1$ D_0	Status Register Read	D7 = 0:reserved D7 = 1:reserved D6 = 0:indicates the display is ON D6 = 1:indicated the display is OFF D5 = 0:reserved D5 = 1:reserved D4 = 0:reserved D4 = 1:reserved

Note
(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

For detailed instruction information, see SSD1325 datasheet .

11 . MPU Interface

Conditions:

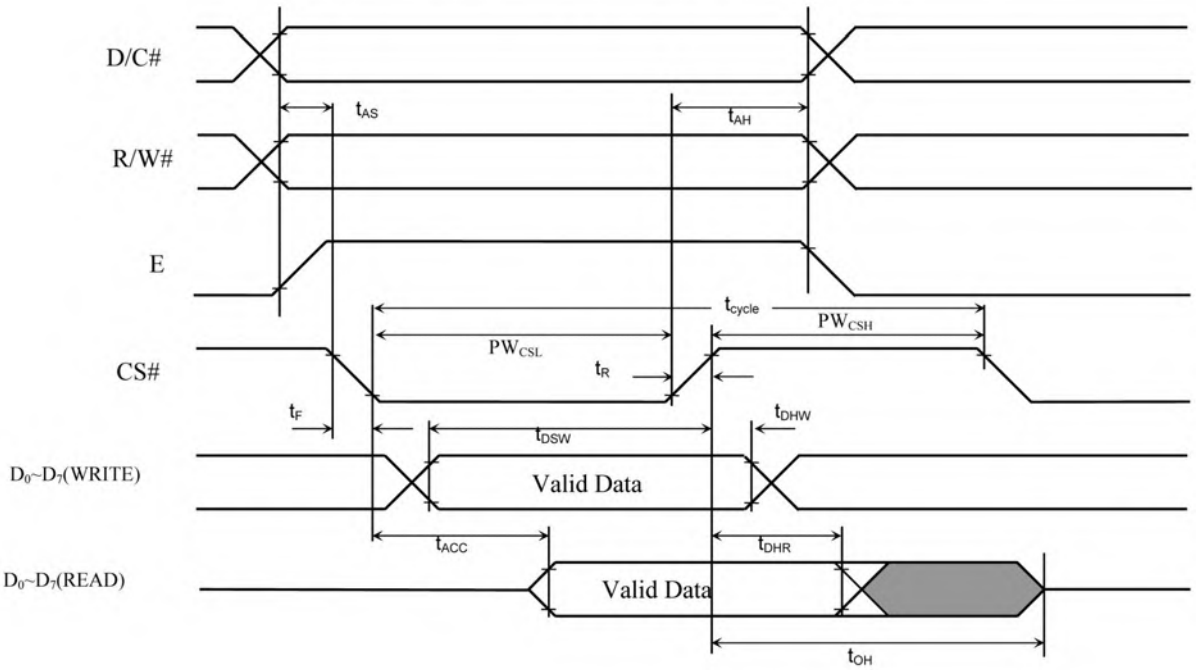
V_{DD} - V_{SS} = 2.4 to 3.5V

T_A = 25°C

Table 25 : 6800-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 34 : 6800-series MCU Parallel Interface Characteristics



Conditions:

V_{DD} - V_{SS} = 2.4 to 3.5V

T_A = 25°C

Table 26 : 8080-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 35 : 8080-series parallel interface characteristics (Form 1)

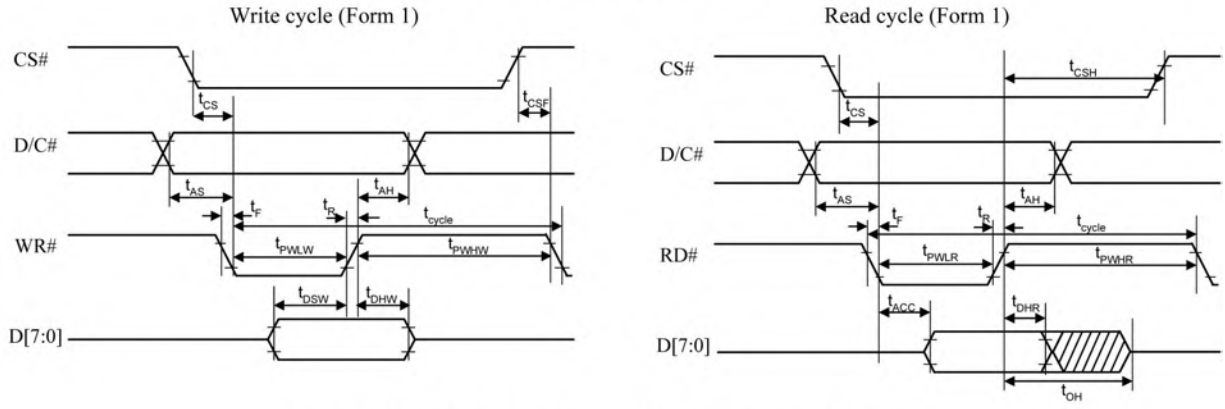
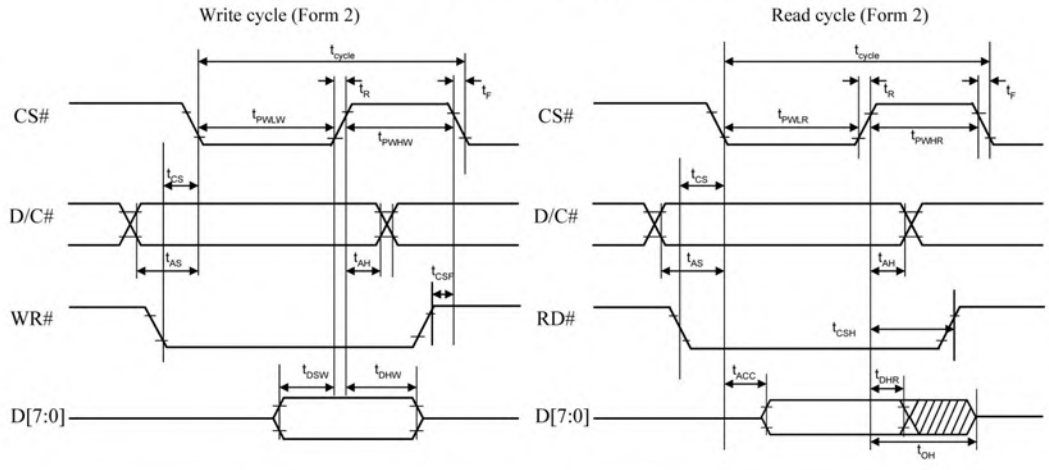


Figure 36 : 8080-series parallel interface characteristics (Form 2)



Conditions:

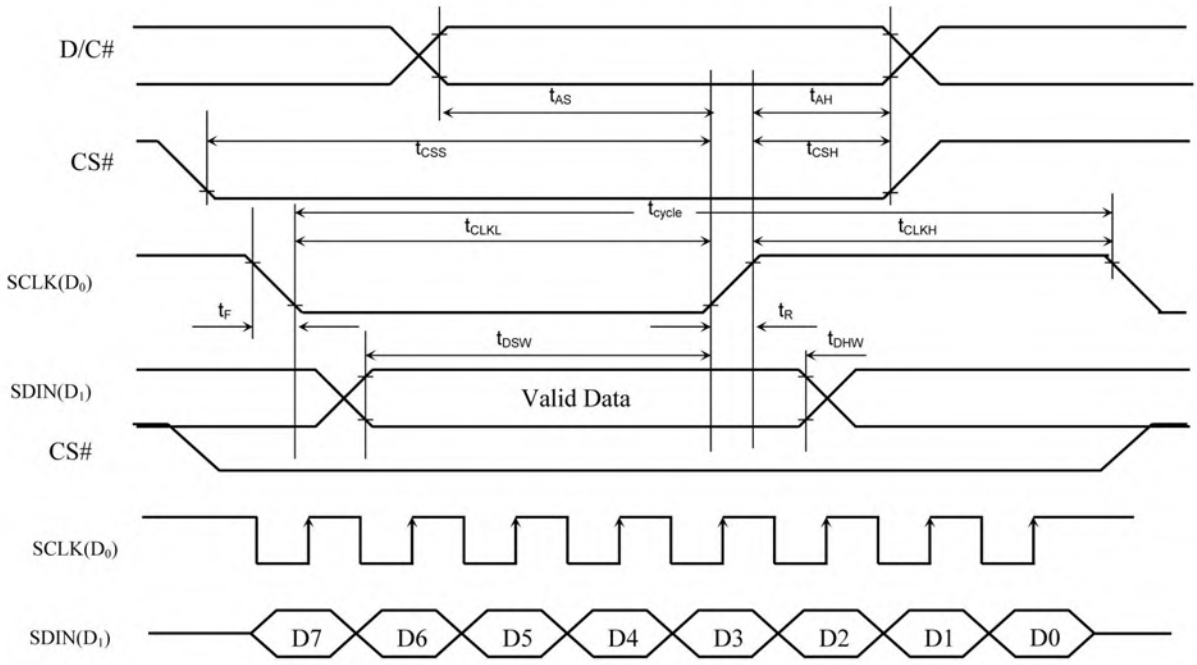
V_{DD} - V_{SS} = 2.4 to 3.5V

T_A = 25°C

Table 27 : Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 37 : Serial Interface Characteristics



12. GDDRAM

12.1 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 11 to Table 15 show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D5117, D5118, D5119 represent the 128x80 data bytes in the GDDRAM.

Table 11 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 11 : GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
⋮	⋮									
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

Table 12 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 12 : GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]
⋮	⋮									
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

Table 13 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  Enable Column Address Re-map (A[0]=1)
  Enable Nibble Re-map (A[1]=1)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 13 : GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|								
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=1

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Table 14 shows the example in which the display start line register is set to 10h with the following condition:

- Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Enable COM Re-map (A[4]=1)
- Display Start Line=10h (corresponds to COM15)
- Data byte sequence: D0, D1, D2 … D5119

Table 14 : GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=10H)

Nibble re-map A[1]=0

Table 15 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  Disable Column Address Re-map (A[0]=0)
  Disable Nibble Re-map (A[1]=0)
  Enable Horizontal Address Increment (A[2]=0)
  Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=4Eh
- Data byte sequence: D0, D1, D2 … D4835

Table 15 : GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
|	|									
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs (Display Startline=0)

Row Address (HEX)

Nibble re-map A[1]=0

Note
(1) Please refer to Table 18 for the details of setting command "Set Re-map"A0h.
(2) The "Display Start Line" is set by the command "Set Display Start Line" A1h and please refer to Table 18 for the setting details
(3) The "Column Start/End Address" is set by the command "Set Column Address" 15h and please refer to Table 18 for the setting details
(4) The "Row Start/End Address" is set by the command "Set Row Address" 75h and please refer to Table 18 for the setting detail

13. Gray Scale Decoder

There are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, GS0 has no pre-charge (phase 2) and no current drive (phase 3). Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

Table16 : Gray scale pulse width set table

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
.	.	.
.	.	.
.	.	.
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

Figure 15 : Gray scale pulse width set diagram

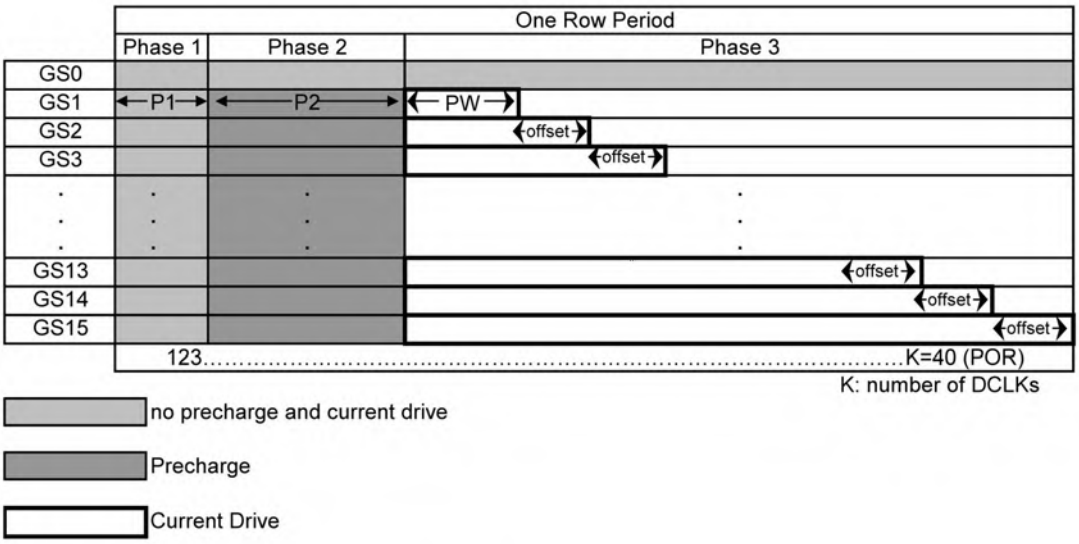


Table 17 : Gray scale pulse width default values

RESET	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29

14 . DESIGN AND HANDING PRECAUTION

14.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

14.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

14.3 Never attempt to disassemble or rework the LCD module.
14.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
14.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
14.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
14.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
14.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
14.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
14.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
14.11 Take care and prevent get hurt by the LCD panel edge.
14.12 Never operate the LCD module exceed the absolute maximum ratings.
14.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
14.14 Never apply signal to the LCD module without power supply.
14.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
14.16 LCD module reliability may be reduced by temperature shock.
14.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module