LOW-VOLTAGE DIGITAL-SIGNAL IC

UCi6963

640x256 Dot Matrix LCD Controller

Preliminary Specifications
Datasheet Revision: 0.7

IC Version: c_A
June 19, 2014

ULTRACHIP

The Coolest LCD Driver, Ever!

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UCi6963

640x256 Dot Matrix LCD Controller IC

INTRODUCTION

The UCi6963 is a dot matrix LCD Controller fully compatible with T6963C. It supports various LCD Driver for standard or custom-made LCD module. The UCi6963 builds in a 256-word CG (Character Generator) ROM for ASCII, Japanese or numeric display in text mode. It also supports Graphics mode and mixed display with Text. The supported maximum external display RAM is 64Kbyte and the display Window can be moved freely within the allocated memory range. The UCi6963 has an 8-bit parallel data bus that can be directly connected to an 8080 series MPU.

The UCi6963 supports a very broad range of LCD formats by allowing selection of different combination of text and graphic modes, including various attribute functions.

MAIN APPLICATOINS

- Industrial Display

FEATURE HIGHLIGHTS

- Support Display Range:
  - Columns: 32, 40, 64, 80
  - Rows: 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32
- Support 8080 8-bit MPU Interface
- Built-in 256-word Font ROM: Basic ASCII, Japanese, Numeric
- Support Max. 64Kbyte External Display SRAM Display Mode : Character, Graphics, and Mixed Mode
- Font Size :
  - Horizontal: 5-, 6-, 7-, 8-pixel
  - Vertical: 8-pixel
- Support Bold Font and Reverse Display
- Support Various LCD Driver
- Support 1/16 ~1/128 Duty
- Built-in X'tal Oscillator or Using External Clock
- Power Supply Range: 3.0~5.5V
- Package: LQFP-67Pin (RoHS Compliance)

ORDERING INFORMATION

Part Number	Description
UCi6963cAULX67YX-E	LQFP-67 pin, RoHS Compliance Package, Font-01
UCi6963cAULX67YX-J	LQFP-67 pin, RoHS Compliance Package, Font-02

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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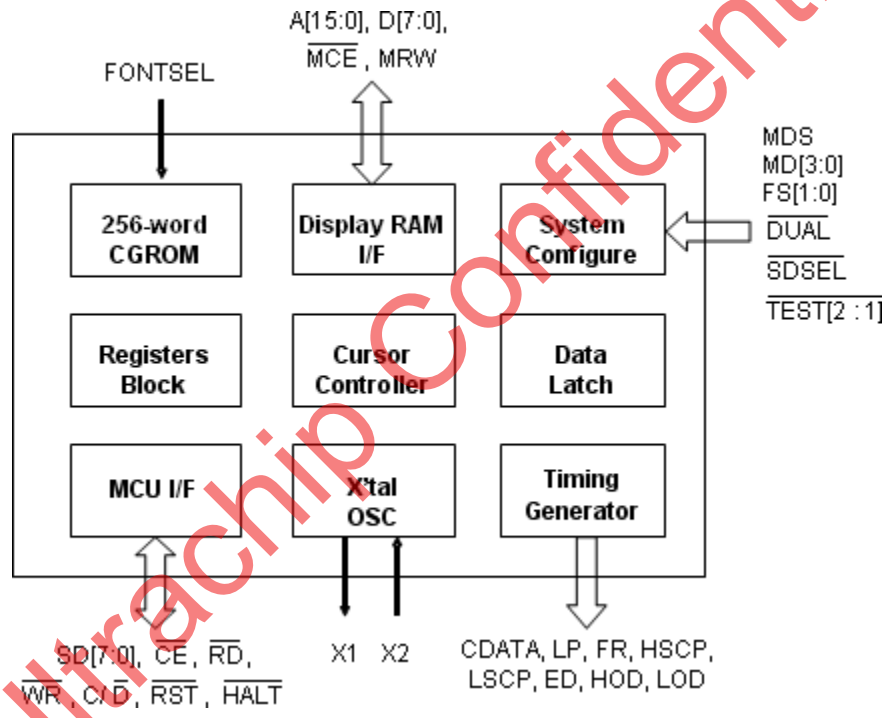
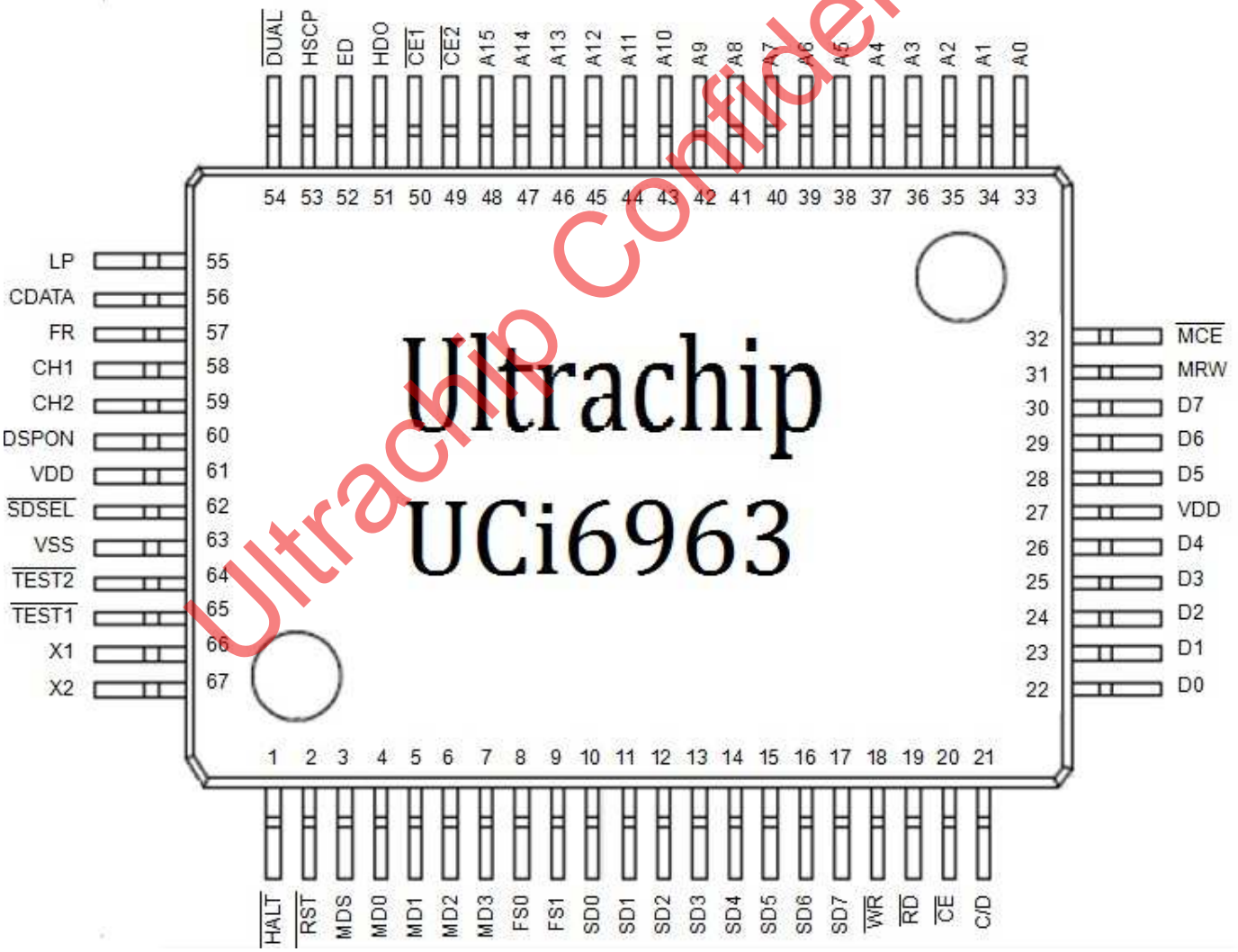
BLOCK DIAGRAM



PIN DESCRIPTION

LQFP-67Pin



Pin (Pad) Name	Pins	Type	Description
MPU Interface			
SD7~SD0	8	I/O	MPU Data Bus, for data transfer between MPU and UCi6963.
$\overline{RD}$ (RDB)	1	I	Data-read signal for Read Control. LOW: MPU reads data from UCi6963.
$\overline{WR}$ (WRB)	1	I	Data-write signal for Write Control. LOW: MPU write data into UCi6963.
C/$\overline{D}$	1	I	Command/Data Select, or Register select. C/$\overline{D}$ = H, $\overline{RD}$ = L: Status-Read C/$\overline{D}$ = H, $\overline{WR}$ = L: Command-Write C/$\overline{D}$ = L, $\overline{RD}$ = L: Data-Read C/$\overline{D}$ = L, $\overline{WR}$ = L: Data-Write
$\overline{CE}$ (CEB)	1	I	Chip Enable. When MPU communicates with UCi6963, this pin must be LOW.
LCD Drive Signals			
FR	1	O	Frame
LP	1	O	Latch Pulse for column driver. Shift clock pulse for Row driver.
CDATA	1	O	Synchronous data for Row Driver.
HSCP	1	O	Shift Clock Pulse for Column driver in upper area of LCD.
HOD	1	O	Data Output for **odd** columns in upper area of LCD.
ED	1	O	Data Output. $\overline{SDSEL}$ = HIGH: Data output for *even* columns in both upper and lower areas of LCD. $\overline{SDSEL}$ = LOW: Data output for columns in both upper and lower area of LCD.
DSPON	1	O	Display ON/OFF control signal. When $\overline{HALT}$ or $\overline{RST}$ is LOW, DSPON outputs LOW and the LCD display is OFF.
Display Memory Control			
A15~A0	16	O	Address output for external memory.
D7~D0	8	I/O	Data bus for external memory.
$\overline{MCE}$ (MCEB)	1	O	Memory Chip Enable LOW: Memory Enable. HIGH: Memory Disable.
MRW	1	O	Memory Read/Write control LOW: Memory Write Enabled. HIGH: Memory Read Enabled.
$\overline{CE0}$ (CEB0)	1	O	Memory Chip Enable 0. $\overline{DUAL}$ = H: Chip enable pin for display memory within the address range: 0000~07FFh $\overline{DUAL}$ = L: Serial data output for odd columns in lower area of LCD.

<table>
<tr><th>Pin (Pad) Name</th><th>Pins</th><th>Type</th><th>Description</th></tr>
<tr><td>$\overline{CE1}$
(CEB1)</td><td>1</td><td>O</td><td>Memory Chip Enable 1.
<table>
<tr><th>$\overline{DUAL}$</th><th>function</th></tr>
<tr><td>H</td><td>Chip enable pin for display memory within the address range: 0800~0FFFh</td></tr>
<tr><td>L</td><td>Shift clock output for column driver in lower are of LCD.</td></tr>
</table></td></tr>
<tr><td>VDD
(VCC)</td><td>2</td><td>P</td><td>Power</td></tr>
<tr><td>GND
(VSS)</td><td>1</td><td>P</td><td>Ground</td></tr>
<tr><th colspan="4">Misc. Pins</th></tr>
<tr><td>$\overline{DUAL}$
(DUALB)</td><td>1</td><td>I</td><td>Scan Selection.
Low: Dual-scan mode. High: Single-scan mode.</td></tr>
<tr><td>MDS,
MD[3:0]</td><td>1
4</td><td>I</td><td>{MDS, MD[1:0]}: LCD Size selection.
<table>
<tr><th>$\overline{DUAL}$</th><th>MDS</th><th>MD1</th><th>MD0</th><th>Lines</th><th>V-dots</th></tr>
<tr><td colspan="6">1 Screen</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>2</td><td>16</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>4</td><td>32</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>6</td><td>48</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>8</td><td>64</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>10</td><td>80</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>L</td><td>12</td><td>96</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>14</td><td>112</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>16</td><td>128</td></tr>
<tr><td colspan="6">2 Screens</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4</td><td>32</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>8</td><td>64</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>12</td><td>96</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>16</td><td>128</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>20</td><td>160</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>24</td><td>192</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>28</td><td>224</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>32</td><td>256</td></tr>
</table>
MD[3:2]: Column selection
<table>
<tr><th>MD3</th><th>MS2</th><th># of Columns</th></tr>
<tr><td>L</td><td>L</td><td>80</td></tr>
<tr><td>L</td><td>H</td><td>64</td></tr>
<tr><td>H</td><td>L</td><td>40</td></tr>
<tr><td>H</td><td>H</td><td>32</td></tr>
</table></td></tr>
<tr><td>X1</td><td>1</td><td>I</td><td>Crystal Oscillator Input. (Threr's a crystal / ceramic oscillator circuit built-in.)
The oscillation frequency is adjusted according to the display size. If using an external clock, use the X1 pin as the clock input. (Leave X2 open.) External capacitors is 15 to 20pF for Crystal or Ceramic oscillator.</td></tr>
<tr><td>X2</td><td>1</td><td>O</td><td>Crystal Oscillator Output</td></tr>
<tr><td>FS[1:0]</td><td>2</td><td>I</td><td>Font Setting.
<table>
<tr><th>FS1</th><th>FS0</th><th>Font</th></tr>
<tr><td>L</td><td>L</td><td>8 x 8</td></tr>
<tr><td>L</td><td>H</td><td>7 x 8</td></tr>
<tr><td>H</td><td>L</td><td>6 x 8</td></tr>
<tr><td>H</td><td>H</td><td>5 x 8</td></tr>
</table></td></tr>
<tr><td>$\overline{SDSEL}$
(SDSELB)</td><td>1</td><td>I</td><td>Data Transfer Mode.
LOW: Sending data by smple serial mode.
HIGH: Sending data by odd/even seperation mode.</td></tr>
</table>

Pin (Pad) Name	Pins	Type	Description
$\overline{\text{HALT}}$ (HALTB)	1	I	Halt Signal. LOW: Stop the Clock HIGH: Normal mode.
$\overline{\text{RST}}$ (RSTB)	1	I	Reset Signal. LOW: the chip will be reset. HIGH: normal mode. There's a built-in Pull-High resistor.
$\overline{\text{TEST[2:1]}}$ (TEST1, TEST2)	2	I	Test Pins. No need to connect.
CH2, CH1	2	O	Check Signals.
FONTSEL	1	I	CGROM Font Set Selection. LOW: select defult CGROM font-01. HIGH: select default CGROM font-02. This pin is reserved for die-based chip only. Connect to Lead Frame.
GND (VSS)	1		Connect to Lead Frame.

Flowchart of Communications with MPU

1. Status Read: A Status Check must be performed before data is read or written.

Status Check. The Status of UCi6963 can be read from the data lines.

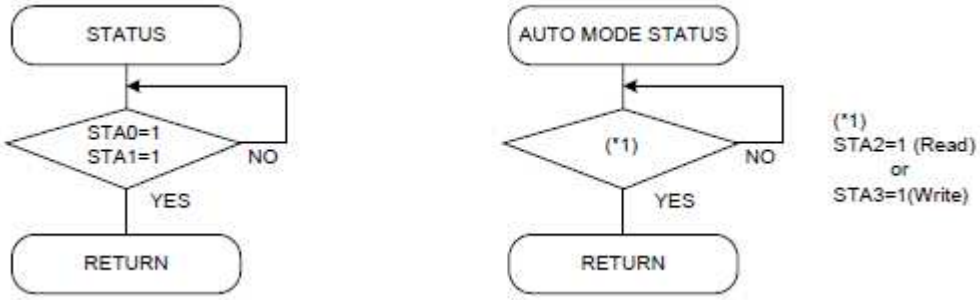
$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	C/$\overline{D}$	SD[7:0]
L	H	L	H	Status Word

MSB			STATUS WORD				LSB
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

STA0: Check command execution capability 0: Disable, 1: Enable
STA1: Check data read/write capability 0: Disable, 1: Enable
STA2: Check Auto mode data read capability 0: Disable, 1: Enable
STA3: Check Auto mode data write capability 0: Disable, 1: Enable
STA4: Not used
STA5: Check controller operation capability 0: Disable, 1: Enable
STA6: Error flag. Used for Screen copy commands. 0: No error, 1: Error
STA7: Check the blink condition 0: Display off, 1: Normal display

(1) It is necessary to check STA0 and STA1 at the same time. There is a possibility of erroneous operation due to a hardware interrupt.
(2) For most modes, STA0 /STA1 are used as a status check.
(3) STA2 and STA3 are valid in Auto mode; STA0 and STA1 are invalid.

Status Checking Flow:



(4) When using the MSB=0 command, a Status Read must be performed.

If a status check is not carried out, the UCi6963 cannot operate normally, even after a delay time.

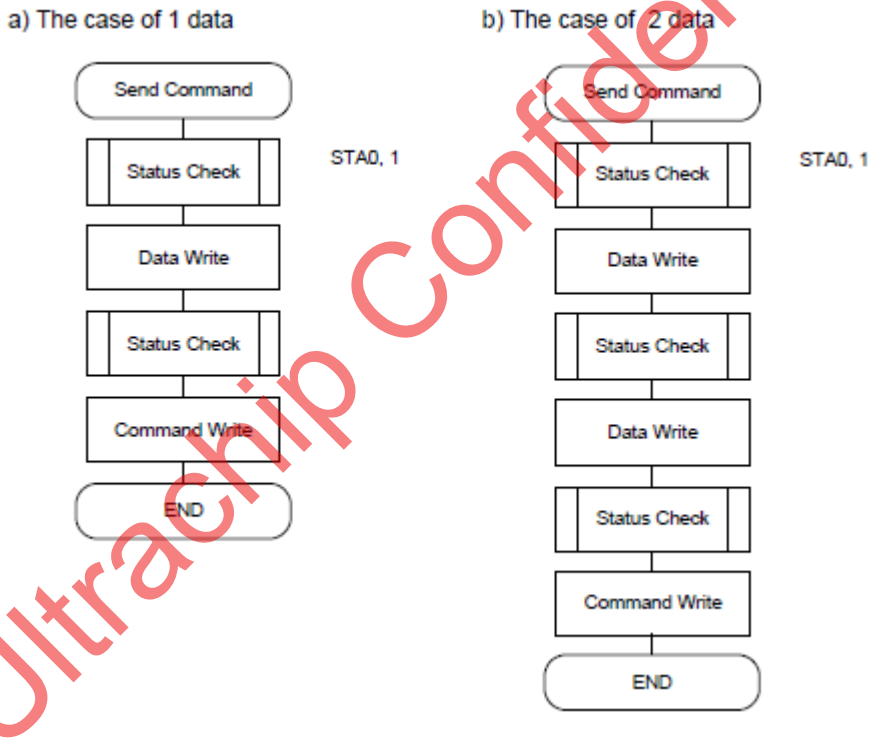
The hardware interrupt occurs during the address calculation period (at the end of each line).

If a MSB=0 command is sent to the UCi6963 during this period, the UCi6963 enters Wait status.

If a status check is not carried out in this state before the next command is sent, there is the possibility that command or data will not be received.

2. Setting Data: When using the UCi6963, first set the data, then set the command.

Procedure for Sending a Command:



When sending more than two data, the last datum (or last two data) is valid.

COMMAND TABLE

C/D: 1: Command / 0: Data W/R: 0: Write Cycle / 1: Read Cycle D7-D0: –: Don't Care / #: Valid data

No.	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Value
1.	Set Cursor Pointer	1	0	0	0	1	0	0	0	0	1		21h
		0	0	#	#	#	#	#	#	#	#	Set X address	
		0	0	#	#	#	#	#	#	#	#	Set Y address	
2.	Set Offset Register	1	0	0	0	1	0	0	0	1	0		22h
		0	0	#	#	#	#	#	#	#	#	Data	
		0	0	0	0	0	0	0	0	0	0		00h
3.	Set Address Pointer	1	0	0	0	1	0	0	1	0	0		24h
		0	0	#	#	#	#	#	#	#	#	Low address	
		0	0	#	#	#	#	#	#	#	#	High address	
4.	Set Text Home Addr.	1	0	0	1	0	0	0	0	0	0		40h
		0	0	#	#	#	#	#	#	#	#	Low address	
		0	0	#	#	#	#	#	#	#	#	High address	
5.	Set Text Area	1	0	0	1	0	0	0	0	0	1		41h
		0	0	#	#	#	#	#	#	#	#	Columns	
		0	0	0	0	0	0	0	0	0	0		
6.	Set Graphic Home Addr.	1	0	0	1	0	0	0	0	1	0		42h
		0	0	#	#	#	#	#	#	#	#	Low address	
		0	0	#	#	#	#	#	#	#	#	High address	
7.	Set Graphic Area	1	0	0	1	0	0	0	0	1	1		43h
		0	0	#	#	#	#	#	#	#	#	Columns	
		0	0	0	0	0	0	0	0	0	0		
8.	OR mode	1	0	1	0	0	0	–	0	0	0		8xh
9.	EXOR mode	1	0	1	0	0	0	–	0	0	1		
10.	AND mode	1	0	1	0	0	0	–	0	1	1		
11.	Text Attribute mode	1	0	1	0	0	0	–	1	0	0		
		0	0	–	–	–	–	#	#	#	#		
12.	Internal CG ROM mode	1	0	1	0	0	0	0	–	–	–		
13.	External CG RAM mode	1	0	1	0	0	0	1	–	–	–		
14.	Display Mode	1	0	1	0	0	1	#	#	#	#	Switch Graphic/Text/Cursor/Blink ON/OFF	9xh
15.	Cursor Pattern Select	1	0	1	0	1	0	0	#	#	#	Set cursor: 1~8-line	Axh
16.	Data-write and Increase ADP	1	0	1	1	0	0	0	0	0	0		C0h
		0	0	#	#	#	#	#	#	#	#	Data	
17.	Data-read and Increase ADP	1	1	1	1	0	0	0	0	0	1		C1h
18.	Data-write and Decrease ADP	1	0	1	1	0	0	0	0	1	0		C2h
		0	0	#	#	#	#	#	#	#	#	Data	
19.	Data-read and Decrease ADP	1	1	1	1	0	0	0	0	1	1		C3h
20.	Data-write and Non-variable ADP	1	0	1	1	0	0	0	1	0	0		C4h
		0	0	#	#	#	#	#	#	#	#	Data	
21.	Data-read and Non-variable ADP	1	1	1	1	0	0	0	1	0	1		C5h
22.	Set Data Auto Write	1	0	1	0	1	1	0	0	0	0		B0h
23.	Set Data Auto Read	1	0	1	0	1	1	0	0	0	1		B1h
24.	Auto Reset	1	0	1	0	1	1	0	0	1	0		B2h
25.	Screen Peek	1	0	1	1	1	0	0	0	0	0		E0h
26.	Screen Copy	1	0	1	1	1	0	1	0	0	0		E8h
27.	Bit Set/Reset	1	0	1	1	1	1	#	#	#	#	Set/Reset Bit 0~7	Fxh
28.	Whole Screen Reverse (Triple-byte command)	1	0	1	1	0	1	0	0	0	0		D0h
		0	0	–	–	–	–	–	–	–	#	0: Normal 1: Reverse	
		0	0	–	–	–	–	–	–	–	–	(Don't Care)	

No.	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Value
29.	Blink Time (Triple-byte command)	1	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		50h
		0	0	–	–	–	–	–	#	#	#	000b: 0.066s 100b: 1s 001b: 0.25s 101b: 1.25s **010b: 0.5s** 110b: 1.5s 011b: 1.75s 111b: 2s	010b
		0	0	–	–	–	–	–	–	–	–	(Don't Care)	
30.	Cursor Auto Moving (Triple-byte command)	1	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		60h
		0	0	–	–	–	–	–	–	–	#	**0: disable** 1: enable	
		0	0	–	–	–	–	–	–	–	–	(Don't Care)	
31.	CGROM Font Select (Triple-byte command)	1	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**		70h
		0	0	–	–	–	–	–	–	#	#	00b: Don't care 01b: Don't care 10b: CGROM Font-01 11b: CGROM Font-02	
		0	0	–	–	–	–	–	–	–	–	(Don't Care)	

COMMAND DESCRIPTION

C/D: 0: Data 1: Command W/R: 0: Write Cycle 1: Read Cycle D7-D0: #: Useful data –: Don't Care

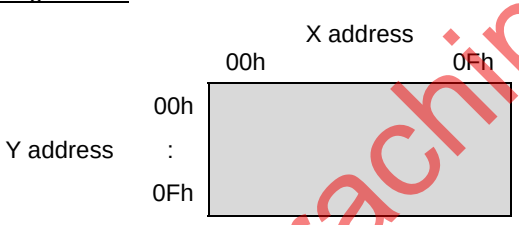
- Register Setting commands:

(1) Set Cursor Pointer (21h)

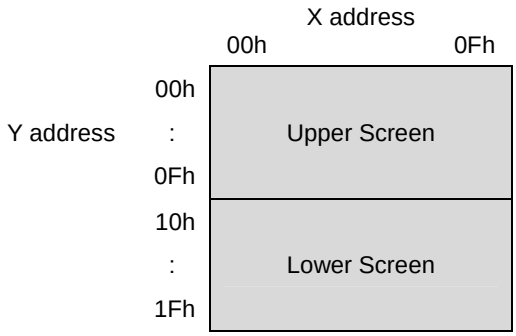
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: (21h)	1:C	0:W	0	0	1	0	0	0	0	1
Set X address: 00h~4Fh	0	0	–	#	#	#	#	#	#	#
Set Y address: 00h~1Fh	0	0	–	–	–	#	#	#	#	#

The X address and Y address specify the position of the cursor. The cursor position can only be moved by this command. Data-read/write from the MPC never changes the cusor pointer. X address and Y address ranges as follows:

Single Scan:



Dual Scan:



(2) Set Offset Register (22h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 22h	1:C	0:W	0	0	1	0	0	0	1	0
	0	0	#	#	#	#	#	#	#	#
00h	0	0	0	0	0	0	0	0	0	0

The UCi6963 has a 16-bit address bus as follows:

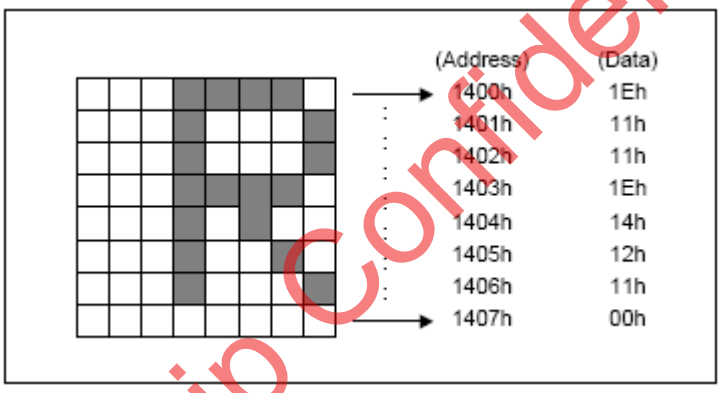
MSB LSB

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Offset Register data					Character code								Line scan		
The 5 MSBs define the start address in external memory of the CG RAM area.					In internal CG ROM mode, 00h ~ 7Fh: predefined "internal" CG ROM characters, 80h ~ FFh: user's own "external" characters. In external CG RAM mode, 00h ~ FFh: user's own characters.									The 3 LSBs indicate one of the eight rows of eight dots that define the character's shape.		

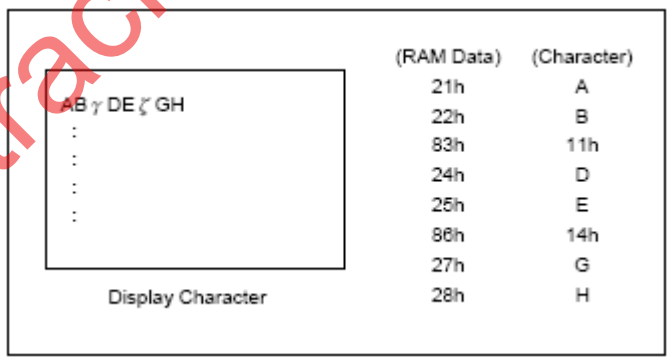
The relationship between Display RAM Address and Offset Register:

Offset Register Data	CG RAM Hex. address (Start to End)
00000	0000 ~ 07FFh
00001	0800 ~ 0FFFh
00010	1000 ~ 17FFh
00011	1800 ~ 1FFFh
:	:
11100	E000 ~ E7FFh
11101	E800 ~ EFFFh
11110	F000 ~ F7FFh
11111	F800 ~ FFFFh

Example 1:
Offset Register : 02h
Character Code: 80h
Character Generator RAM Start address: 0001b (=1h), 0100b (=4h), 0000b (=0h), 0000b (=0h)



Example 2:
The relationship between Display RAM data and display characters :



The γ and ζ are displayed by character generator RAM.

(3) Set Address Pointer (24h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 24h	1:C	0:W	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**
Low address	0	0	#	#	#	#	#	#	#	#
High address	0	0	#	#	#	#	#	#	#	#

The Set Address Pointer command is used to indicate the start address for writing to (or reading from) External RAM.

Flow: Status check → Set Address Data (lower 8 bits) → Status check → Set Address Data (upper 8 bits) → Status check → Set Address Pointer

■ Control word Setting commands: The home address and column size are defined by the following commands:

(4) Set Text Home Address (40h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 40h	1:C	0:W	0	1	0	0	0	0	0	0
Low address	0	0	#	#	#	#	#	#	#	#
High address	0	0	#	#	#	#	#	#	#	#

The starting address in the external display RAM for text display is defined by this command. The Text Home Address indicates the leftmost and uppermost position.

The Relationship between Display RAM Address and Display Position :

Display RAM Address		Display Position
TH	...	TH + CL
TH + TA	...	TH + TA + CL
(TH + 2TA) + TA	...	TH + 2TA + CL
(TH + 3TA) + TA	...	TH + 3TA + CL
:	:	:
TH + (n+1) TA	...	TH + (n-1) TA + CL

Remark: TH: Text Home address
TA: Text Area number (columns)
CL: Columns are fixed by hardware (pin-programmable).

Example:
Text Home address: 0000h
Text Area: 0020h
MD2=H, MD3=H: 32 columns
$\overline{\text{DUAL}}$ =H, MDS=L, MD0=L, MD1=H: 4 lines

0000h	0001h	... ...	001Eh	001Fh
0020h	0021h	... ...	003Eh	003Fh
0040h	0041h	... ...	005Eh	005Fh
0060h	0061h	... ...	007Eh	007Fh

(5) Set Text Area (41h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 41h	1:C	0:W	0	1	0	0	0	0	0	1
Set Columns	0	0	#	#	#	#	#	#	#	#
00h	0	0	0	0	0	0	0	0	0	0

The display columns are defined by the hardware setting. This command can be used to adjust the columns fo the display.

Example:
LCD Size: 20 columns, 4 lines
Text Home Address: 0000h
Text Area: 0014h
MD2=H, MD3=H: 32 columns
$\overline{\text{DUAL}}$ =H, MDS=L, MD0=L, MD1=H: 4 lines

0000	0001	.....	0013	0014	.....	001F
0014	0015	.....	0027	0028	.....	0033
0028	0029	.....	003B	003C	.....	0047
003C	003D	.....	004F	0050	.....	005B

(6) Set Graphic Home Address (42h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 42h	1:C	0:W	0	1	0	0	0	0	1	0
Set Low address	0	0	#	#	#	#	#	#	#	#
Set High address	0	0	#	#	#	#	#	#	#	#

The starting address of the external display RAM used for graphic display is defined by this command. The graphic home address indicates the leftmost and uppermost position.

The Relationship between External Display RAM Address and Display Position:

GH	.....	GH + CL
GH + GA	.....	GH + GA + CL
(GH + GA) + GA	.....	GH + 2GA + CL
(GH + 2GA) + GA	.....	GH + 3GA + CL
⋮	⋮	⋮
GH + (n-1) GA	.....	GH + (n-1) GA + CL

Remark: GH: Graphic Home Address
GA: Graphic Area Number (columns)
CL: Columns are fixed by hardware (pin-programmable).

Example:
Graphic Home Address: 0000h
Graphic Area: 0020h
MD2=H, MD3=H: 32 columns
$\overline{\text{DUAL}}$ =H, MDS=L, MD0=H, MD1=H: 2 lines

0000h	0001h	.....	001Eh	001Fh
0020h	0021h	.....	003Eh	003Fh
0040h	0041h	.....	005Eh	005Fh
0060h	0061h	.....	007Eh	007Fh
0080h	0081h	.....	009Eh	009Fh
00A0h	00A1h	.....	00BEh	00BFh
00C0h	00C1h	.....	00DEh	00DFh
00E0h	00E1h	.....	00FEh	00FFh
0100h	0101h	.....	011Eh	011Fh
0120h	0121h	.....	013Eh	013Fh
0140h	0141h	.....	015Eh	015Fh
0160h	0161h	.....	017Eh	017Fh
0180h	0181h	.....	019Eh	019Fh
01A0h	01A1h	.....	01BEh	01BFh
01C0h	01C1h	.....	01DEh	01DFh
01E0h	01E1h	.....	01FEh	01FFh

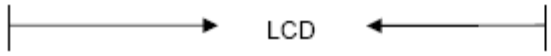
(7) Set Graphic Area (43h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 43h	1:C	0:W	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
Set # of Columns	0	0	#	#	#	#	#	#	#	#
00h	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

The display columns are defined by the hardware setting. This command can be used to adjust the columns of the graphic display.

Example:
LCD Size : 20 columns, 2 lines
Graphic Home Address : 0000h
Graphic Area : 0014h
MD2=H, MD3=H : 32 columns
$\overline{\text{DUAL}}$ =H, MDS=L MD0=H, MD1=H : 2 lines

0000	0001	.....	0013	0014	.....	001F
0014	0015	.....	0027	0028	.....	0033
0028	0029	.....	003B	003C	.....	0047
003C	003D	.....	004F	0050	.....	005B
0050	0051	.....	0063	0064	.....	006F
0064	0065	.....	0077	0078	.....	0083
0078	0079	.....	008B	008C	.....	0097
008C	008D	.....	009F	00A0	.....	00AB
00A0	00A1	.....	00B3	00B4	.....	00BF
00B4	00B5	.....	00C7	00C8	.....	00D3
00C8	00C9	.....	00DB	00DC	.....	00E7
00DC	00DD	.....	00EF	00F0	.....	00FD
00F0	00F1	.....	0103	0104	.....	011F
0104	0105	.....	0127	0128	.....	0123
0128	0129	.....	013B	013C	.....	0147
013C	013D	.....	014F	0150	.....	015B



If the graphic setting is set to match the desired number of columns on the LCD, the addressing scheme will be automatically modified so that (the start address of each line) = (the end address of the previous line) +1.

■ Mode Setting commands: The display mode is defined by the following commands. The display mode does not change until the next command is sent.

(8) OR mode (80h/88h)

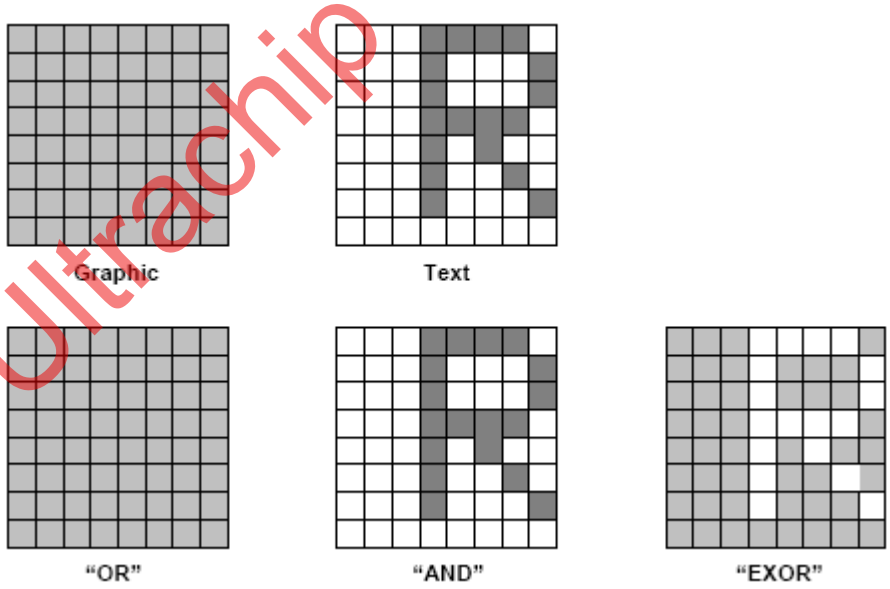
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 80h or 88h	1:C	0:W	1	0	0	0	–	0	0	0

(9) EXOR mode (81h/89h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 81h or 89h	1:C	0:W	1	0	0	0	–	0	0	1

(10) AND mode (83h/8Bh)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 83h or 8Bh	1:C	0:W	1	0	0	0	–	0	1	1



Note: The logical OR, EXOR, and AND can be applied to either text or graphic display.

(11) Text Attribute mode (84h/8Ch)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 84h or 8Ch	1:C	0:W	1	0	0	0	–	1	0	0
Set Inhibit / Reverse / Bold / Blink	0	0	–	–	–	–	#	#	#	#

The attribute operations are to choose the combination of Reverse display, Character blink, bold and Inhibit. Only text display is possible in Attribute Function mode; graphic display is automatically disabled. However, the Display Mode command must be used to turn ON both Text and Graphic areas to make the Attribute function available.

The attribute data for each character in the text area is written to the same address in the graphic area.

D[3:0]:

0000b: Normal Display
0011b: Inhibit Display
0101b: Reverse Display
0111b: Bold Display
1000b: Blink of Normal Display
1011b: Blink of Inhibit Display
1101b: Blink of Reverse Display
1111b: Blink of Bold Display

Note: Attribute functions can only be applied to text display, since the attribute data are placed in the graphic RAM area.

(12) Internal CG ROM mode (80h~87h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Select the Internal CG ROM mode	1:C	0:W	1	0	0	0	0	–	–	–

This command selects the Internal CG ROM mode. In the Internal Character Generator mode, character codes 00h to 7Fh are assigned to the built-in Character generator ROM.

00h ~ 7Fh: predefined "internal" CG ROM characters,
80h ~ FFh: user's own "external" characters.

(13) External CG RAM mode (88h~8Fh)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Select the External CG RAM mode	1:C	0:W	1	0	0	0	1	–	–	–

This command selects the External CG RAM mode. In this mode, character codes 80h to FFh are automatically assigned to the external character generator RAM.

■ Display mode Setting command:

(14) Display Mode (90h~9Fh)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Graphic/Text/Cursor/Blink ON/OFF	1:C	0:W	1	0	0	1	–	–	–	–

The display mode is defined by this command and does not change until the next command is sent. The logical OR, EXOR, AND of text or graphic display can be displayed.

	D3: Graphic Display	D2: Text Display	D1: Cursor Display	D0: Cursor Blink
0b	OFF	OFF	OFF	OFF
1b	ON	ON	ON	ON

D[3:0]: 0000b: Display OFF
01xxb: Text ON, Graphic OFF
xx10b: Cursor ON, Blink OFF
10xxb: Text OFF, Graphic ON
xx11b: Cursor ON, Blink ON
11xxb: Text ON, Graphic ON

Note: It's necessary to turn ON "Text display" and "Graphic display" in the following cases:
a) Combination of text/graphic display
b) Attribute function

■ Cursor Pattern Selection command:

(15) Cursor Pattern Select (A0h~A7h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Select Cursor Height	1:C	0:W	1	0	1	0	0	#	#	#

When cursor display is ON, this command selects the cursor pattern in the range 1 line to 8 lines. The cursor address is defined by the Cursor pointer Set command.

D[2:0]: 000b: 1-line cursor
001b: 2-line cursor
010b: 3-line cursor
011b: 4-line cursor
100b: 5-line cursor
101b: 6-line cursor
110b: 7-line cursor
111b: 8-line cursor

■ Data-Read/-Write commands: These commands are used for writing data from the MPU to external display RAM, and reading data from external display RAM. Data-Write / Data-Read should be executed after setting address using Set Address Pointer command. The address pointer can be automatically incremented or decremented using this command.

Note: This command is necessary for each 1-byte datum.

(16) Data-write and Increase ADP (C0h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C0h	1:C	0:W	1	1	0	0	0	0	0	0
Write Data	0	0	#	#	#	#	#	#	#	#

Address Pointer (ADP) will be increased after the Data-Write action.

Flow: Set Address Pointer (Example Address Pointer=1000h) → Status Check 1 → Set Write Data (Example data=AAh) → Status Check 1 → Data Write (C0h) (AAh is written to Address 1000h and then Address Pointer points to 1001h.)

(17) Data-read and Increase ADP (C1h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C1h	1:C	0:W	1	1	0	0	0	0	0	1

Data will be read to a specific register automatically and the Address Pointer (ADP) will be increased after the Data-Read action.

(18) Data-write and Decrease ADP (C2h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C2h	1:C	0:W	1	1	0	0	0	0	1	0
Write Data	0	0	#	#	#	#	#	#	#	#

Address Pointer (ADP) will be decreased after the Data-Write action.

(19) Data-read and Decrease ADP (C3h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C3h	1:C	0:W	1	1	0	0	0	0	1	1

Data will be read to a specific register automatically and the Address Pointer (ADP) will be decreased after the Data-Read action.

(20) Data-write and Non-variable ADP (C4h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C4h	1:C	0:W	1	1	0	0	0	1	0	0
Write Data	0	0	#	#	#	#	#	#	#	#

Address Pointer (ADP) will not change after the Data-Write action.

(21) Data-read and Non-variable ADP (C5h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: C5h	1:C	0:W	1	1	0	0	0	1	0	1

Data will be read to a specific register automatically and the Address Pointer (ADP) will not change after the Data-Read action.

■ Data-Auto-Read/-Write commands:

(22) Set Data Auto Write (B0h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: B0h	1:C	0:W	1	0	1	1	0	0	0	0

Flow: Set Address Pointer → Status Check 1 → Auto Write (B0h) → Status Check 2 → Data Write → Status Check 2 → Data Write → Status Check 2 → Auto Reset (B2h)

(23) Set Data Auto Read (B1h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: B1h	1:C	0:W	1	0	1	1	0	0	0	1

Flow: Set Address Pointer → Status Check 1 → Auto Read (B1h) → Status Check 2 → Data Read → Status Check 2 → Data Read → Status Check 2 → Auto Reset (B2h)

(24) Auto Reset (B2h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: B2h	1:C	0:W	1	0	1	1	0	0	1	0

■ Screen Peek command:

(25) Screen Peek (E0h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: E0h	1:C	0:W	1	1	1	0	0	0	0	0

This command is used to transfer 1 byte of displayed data to the data stack; this byte can be read from the MPU by data access. The logical combination of text and graphic display data on the LCD screen can be read by this command.

The status (STA6) should be checked just after the Screen Peek command. If the address Determined by the Set Address Pointer command is not in the graphic area, this command is ignored and a status flag (STA6) is set.

Flow: Set Address Pointer → Status Check 1 → Screen Peek (E0h) → Status Check → Status Check 1 → Data Access

Note: This command is available when hardware column number and software column number are the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

■ Screen Copy command:

(26) Screen Copy (E8h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: E8h	1:C	0:W	1	1	1	0	1	0	0	0

This command copies a single raster line of data to the graphic area. The start point must be set using the Set Address Pointer command.

Note 1: If the attribute function is being used, this command is not available. (With Attribute data is graphic area data.)

Note 2: With Dual-Scan, this command cannot be used (because the UCi6963 cannot separate the upper screen data and the lower screen data).

Flow: Set Address Pointer → Status Check 1 → Screen Copy (E8h) → Status Check (whether STA6=1) → Status Check (whether STA0/1=1)

Note: This command is available when hardware column number is the same. Hardware column number is related to MD2 and MD3 setting. Software column number is related to Set Text Area and Set Graphic Area command.

■ Bit Set/Reset command:

(27) Bit Set/Reset (Fxh)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Select Set/Reset & Bit number	1:C	0:W	1	1	1	1	#	#	#	#

This command set or reset a bit of the byte specified by the address pointer. Only one bit can be set / reset at a time.

D[3]: 0: Reset 1: Set
D[2:0]: 000b~111b: Bit 0~7

Flow: Set Address Pointer → Status Check 1 → Bit Set (Reset)

■ Screen Reverse commands:

(28) Whole Screen Reverse (D0h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: D0h	1:C	0:W	1	1	0	1	0	0	0	0
Select Normal / Reverse	0	0	–	–	–	–	–	–	–	#
Dummy Write	0	0	–	–	–	–	–	–	–	–

0: Normal 1: Reverse

This command (D0h) is used to reverse the displayed data of the whole screen. When this function is enabled, the displayed data on the LCD are reversed to show reversing pattern.

■ Blink time commands:

(29) Blink Time (50h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 50h	1:C	0:W	0	1	0	1	0	0	0	0
Select Blink Time	0	0	–	–	–	–	–	#	#	#
Dummy Write	0	0	–	–	–	–	–	–	–	–

The blink time of the blink functions are adjusted by this command (50h). For example, if the frequency of the frame equals 60Hz, the blink time can be adjusted from 0.066 second to 2 second by using software selections.

000: 0.066s 001: 0.25s **010: 0.5s** 011: 0.75s
100: 1s 101: 1.25s 110: 1.5s 111: 2s

Note: In this function, two data must be sent before sending the command, but the content of the second datum (D2) can be any value.

■ Cursor Auto Moving command:

(30) Cursor Auto Moving (60h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 60h	1:C	0:W	0	1	1	0	0	0	0	0
Set Cursor Auto Mov. mode ON/OFF	0	0	–	–	–	–	–	–	–	#
Dummy Write	0	0	–	–	–	–	–	–	–	–

The UCi6963 provides a unique function for the automatic cursor movement. After writing (reading) each displayed datum, the cursor pointer is automatically increased/decreased by one in the Cursor Auto-Moving mode.

0: disable 1: enable

Note: In this function, it must be sent two data before sending the command, but the contents of the second datum (D2) can be any values.

■ CGROM Font Select command:

(31) CGROM Font Select (70h)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write command code: 70h	1:C	0:W	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
Select CGROM Font set	0	0	–	–	–	–	–	–	#	#
Dummy Write	1	0	–	–	–	–	–	–	–	–

This command (70h) is a convenient function for selecting the Character Font Map. The user can get more built-in characters from CGROM Font-01 or CGROM Font-02, which is determined by software selections.

00: Don't care 01: Don't care 10: CGROM Font-01 11: CGROM Font-02

Note: In this function, it must be sent two data before sending the command, but the contents of the second datum (D2) can be any values.

Comparison Table

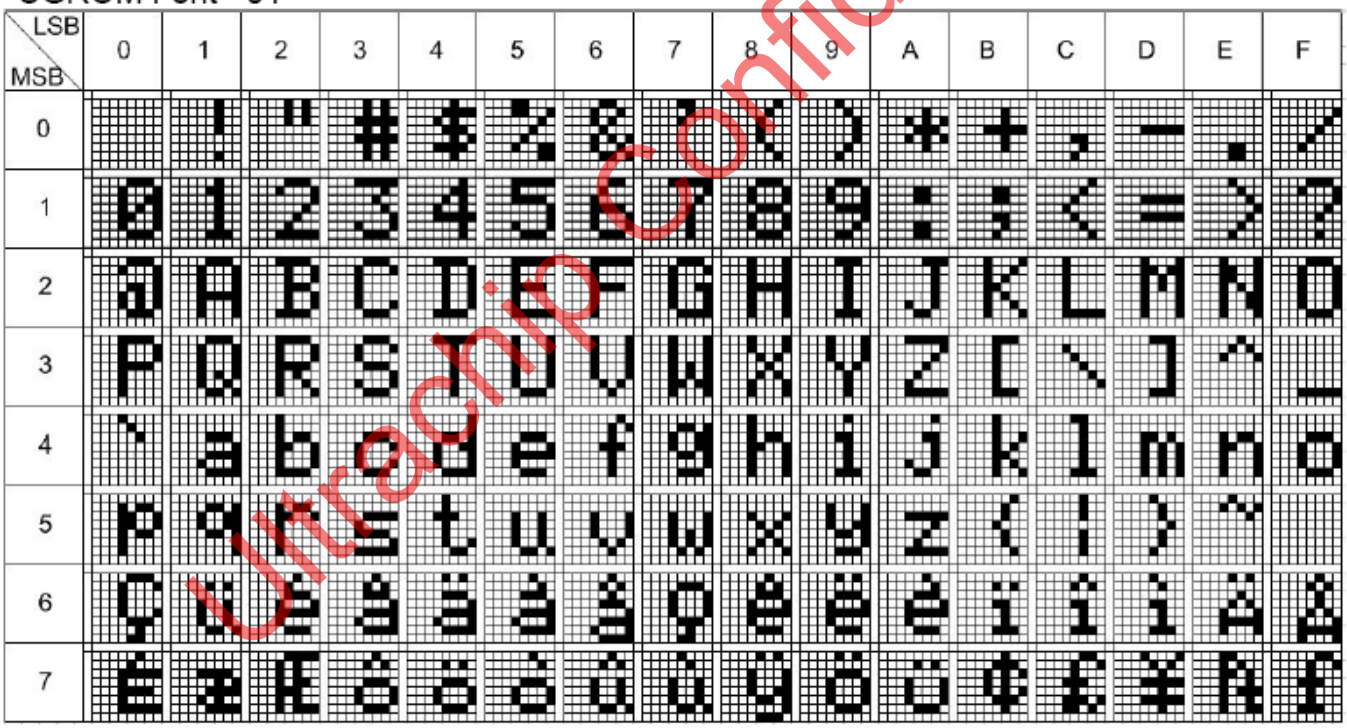
#	Item	Description	ULTRACHIP UCi6963	Toshiba T6963C
1	CGROM Font Select	UCi6963 provides two CGROMs Font-01 and Font-02 *	Yes	–-
2	Blink Time Selection	UCi6963 provides eight selections for blinking	Yes	–-
3	Cursor Auto Move		Yes	–-
4	Whole Screen Reverse		Yes	–-
5	Bold Text and Blink	UCi6963 provides Bold Text feature	Yes	–-
6	Package		LQFP-67pin	LQFP-67pin

* For the detail of CGROM Font sets, see the tables on the following page.

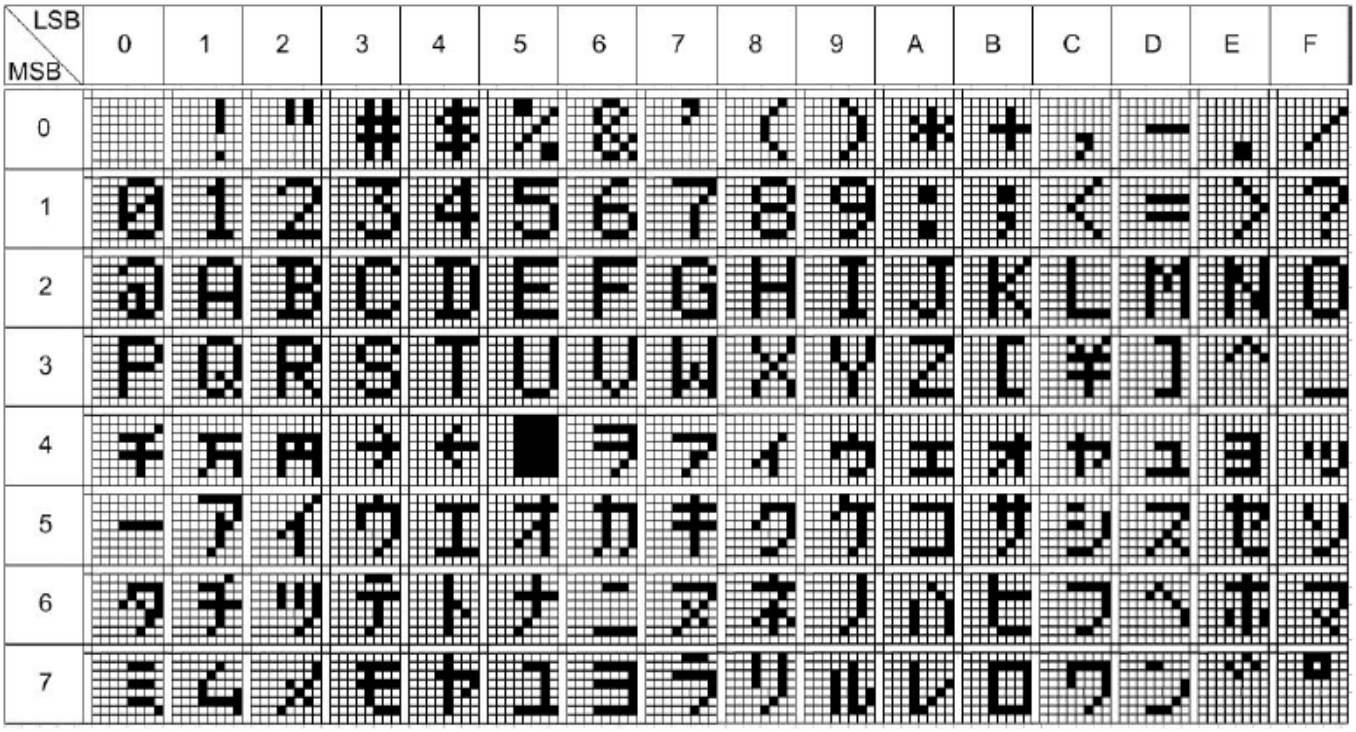
The UCi6963c has 2 part numbers – UCi6963cAULX67YX-E and UCi6963cAULX67YX-J.
The UCi6963cAULX67YX-E is compatible to T6963C (code 0101) and the default font is as the figure shown above.
The UCi6963cAULX67YX-J is compatible to T6963C (code 0201) and the default font is as the figure shown below.

Although UCi6963c provide an extra internal command for MCU to select both font groups, it's not necessary to change the software to select the font if you chose the right part number.

CGROM Font - 01



CGROM Font – 02



FUNCTION DESCRIPTION

Definition

- After power on, it is necessary to reset. The $\overline{RST}$ is kept Low between 5 clocks up (oscillation clock).
- When $\overline{HALT}$ = Low, the oscillation stops. The power supply for the LCD must be turned off, to protect the LCD from DC bias.
- The $\overline{HALT}$ function ($\overline{HALT}$ = Low) includes the RESET function ($\overline{RST}$ =Low).
- The column/line counter and display register are cleared by $\overline{RST}$. (Other registers are not cleared.)
- Disable the display using the clear-display register.
- The status must be checked before data or commands are sent. The MSB=0 status check must be done in particular. There is a possibility of erroneous operation due to a hard interrupt.
- STA0 and STA1 must be checked at the same time. When a command is executed, data transmission errors may occur.
- The UCi6963 can only handle one byte per machine cycle (16 clocks). It is impossible to send more than two data in a machine cycle.
- When using a command with operand data, it important to send the data first, and then executes the command.
- The character fonts used by the UCi6963 are different from ASCII codes.

State after HALT/RESET

Pins	HALT	RESET
SD[7:0]	Floating	Floating
D[7:0]	Floating	Floating
MRW	HIGH	HIGH
$\overline{MCE}$	HIGH (Note 1)	HIGH (Note 1)
A[15:0]	HIGH (Note 2)	HIGH (Note 2)
$\overline{CE1}$, $\overline{CE0}$	HIGH (Note 1)	HIGH (Note 1)
ED, HOD	Final data	Final data
HSCP	LOW	LOW
LP	LOW	LOW
CDATA	HIGH	HIGH
FR	HIGH	HIGH
CH1	LOW	Test Signal
CH2	LOW	Test Signal
DSPON	LOW	LOW
X2	HIGH	OSC Clock
Note 1: In Attribute mode, it's HIGH or LOW according to the state of graphic pointer.		
Note 2: In Attribute mode, it's data-to-graphic pointer.		

Row / Column and Oscillation Clock

The frequency of the crystal oscillator is adjusted by the following formula.

$$\frac{8M}{fscp} x8N = \frac{1}{fR} \quad \text{--> fosc=fR x 64 x 2 x M x N --> fR=60Hz}$$

where fosc: Frequency of Oscillation

fscp: Frequency of shift clock, (fscp=fosc / 2)

fR: Frequency of Frame

M: Number of characters on one line, (number of dots on one line = 8M)

N: Number of rows, (Duty=1/8 N)

Unit: MHz

N		M				Duty
		32	40	64	80	
2	Upper	0.492	0.614	0.983	1.229	1/16
	Lower	0.983	1.229	1.966	2.458	
4	Upper	0.983	1.229	1.966	2.458	1/32
	Lower	1.966	2.458	3.932	4.915	
6	Upper	1.475	1.843	2.949	3.688	1/48
	Lower	2.949	3.685	5.898	7.372	
8	Upper	1.966	2.458	3.932	4.915	1/64
	Lower	3.932	4.915	7.864	9.830	
10	Upper	2.458	3.072	4.915	6.144	1/80
	Lower	4.915	6.144	9.830	12.288	
12	Upper	2.949	3.686	5.898	7.373	1/96
	Lower	5.898	7.373	11.776	14.746	
14	Upper	3.440	4.300	6.881	8.602	1/112
	Lower	6.881	8.601	13.763	17.203	
16	Upper	3.932	4.915	7.864	9.830	1/128
	Lower	7.864	9.830	15.729	19.660	

Remark: Upper: Single scan
Lower: Dual scan at fR=60Hz

RAM Interface

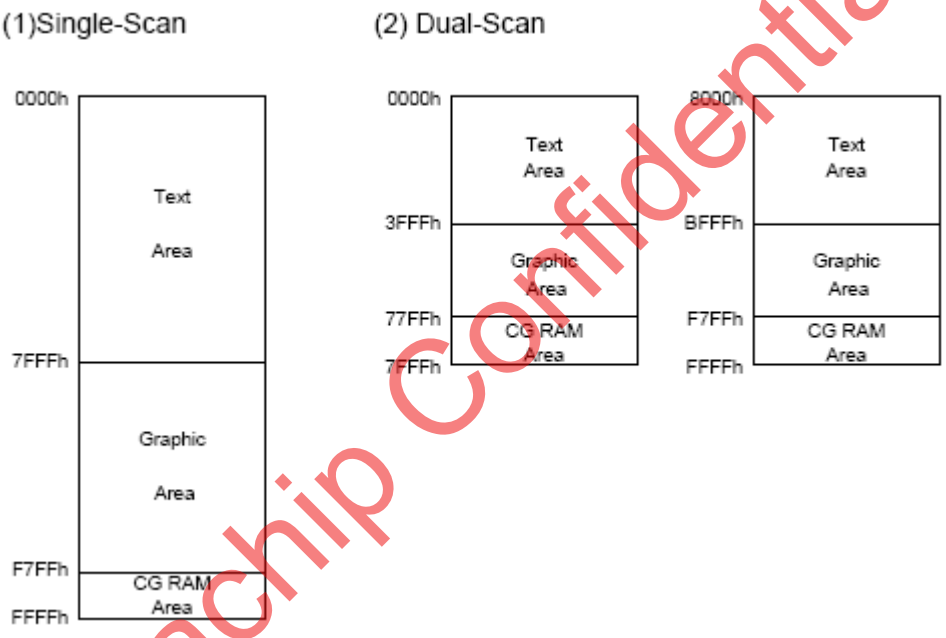
The external RAM is used to store display data (text, graphic and external CG data).

With single-scan, text data, graphic data and external CG data can be freely allocated to the memory area (64 KB max).

With dual-scan, LCD-I is allocated to 0000h to 7FFFh (32 KB max), LCD-II is allocated to 8000h to FFFFh (32-KB Max). Text data, graphic data and external CG data can be freely allocated in LCD-I. In LCD-II, the same addresses must be allocated as in LCD-I, except A15. A15 determines selection of LCD-I or LCD-II.

It can be used the address-decoded signals $\overline{CE0}$ (0000h to 07FFh), $\overline{CE1}$ (0800h to 0FFFh) within 4 KB. $\overline{CE0}$ and $\overline{CE1}$ allow decoding of addresses in the ranges (0000h to 07FFh) and (0800h to 0FFFh) respectively within a 4-KB memory space.

(Example)



ABSOLUTE MAXIMUM RATINGS

GND=0V, Ta=25°C

Signal	Item	Rating	Unit
VDD	Supply voltage range	–0.3 ~ +7.0	V
VIN	Input voltage range	–0.3 ~ VDD+0.3	V
tOP	Operating temperature range	–30 ~ +85	°C
tSTG	Storage temperature range	–55 ~ +125	°C
tSOLDER	Soldering temperature range, Solder Time=8 Min.	400	°C

DC CHARACTERISTICS

(V_{DD}=3.0V~5.5V, V_{SS}=0V, T_A=–20~75°C)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_{IH}	High-level input voltage		0.8 V_{DD}	–	V_{DD}	V
V_{IL}	Low-level input voltage		0	–	0.2 V_{DD}	V
V_{OH}	High-level output voltage		V_{DD}-0.3	–	V_{DD}	V
V_{OL}	Low-level output voltage		0	–	0.3	V
R_{OH}	Output Resistance – HIGH	V_{OUT}=V_{DD}-0.5	–	–	400	Ω
R_{OL}	Output Resistance – LOW	V_{OUT}=0.5	–	–	400	Ω
$I_{DD}1$	Current consumption – Operating	V_{DD} = 5.0V Note (2) fosc=4.0MHz	–	3.0	5	mA
$I_{DD}2$	Current consumption – Halt	V_{DD} = 5.0V	–	1	2	uA
R_{PU}	Input Pull-Up Resistance	Note (1)	50	100	300	KΩ
fosc	Operating Frequency		0.4	6/8	–	MHz
T_{SDT}	Solder Temperature	Solder Time = 20~40 Seconds	–	260	–	°C

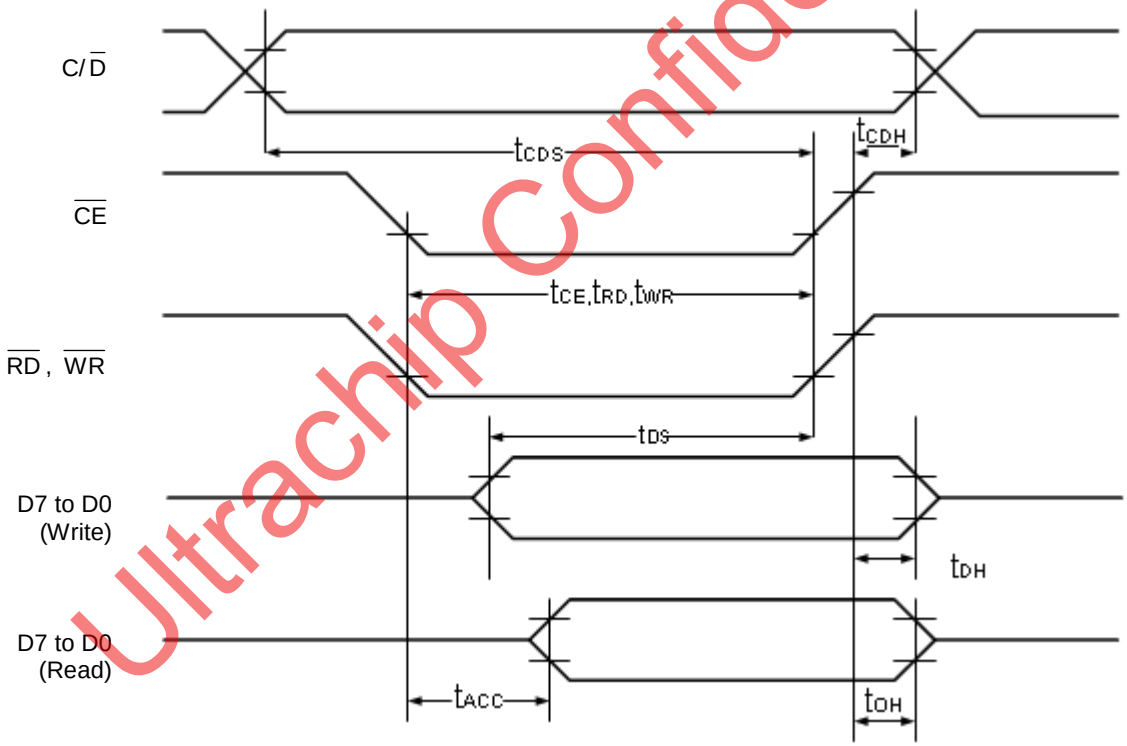
Note:

(1) Applied to $\overline{TEST}$[2:1], $\overline{RST}$

(2) MDS=L, MD[1:0]=LL, MD[3:2]=HH, FS[1:0]=LL, $\overline{SDSEL}$ =L, $\overline{DUAL}$ =H, D[7:0]=LHLHLHLH.

AC CHARACTERISTICS

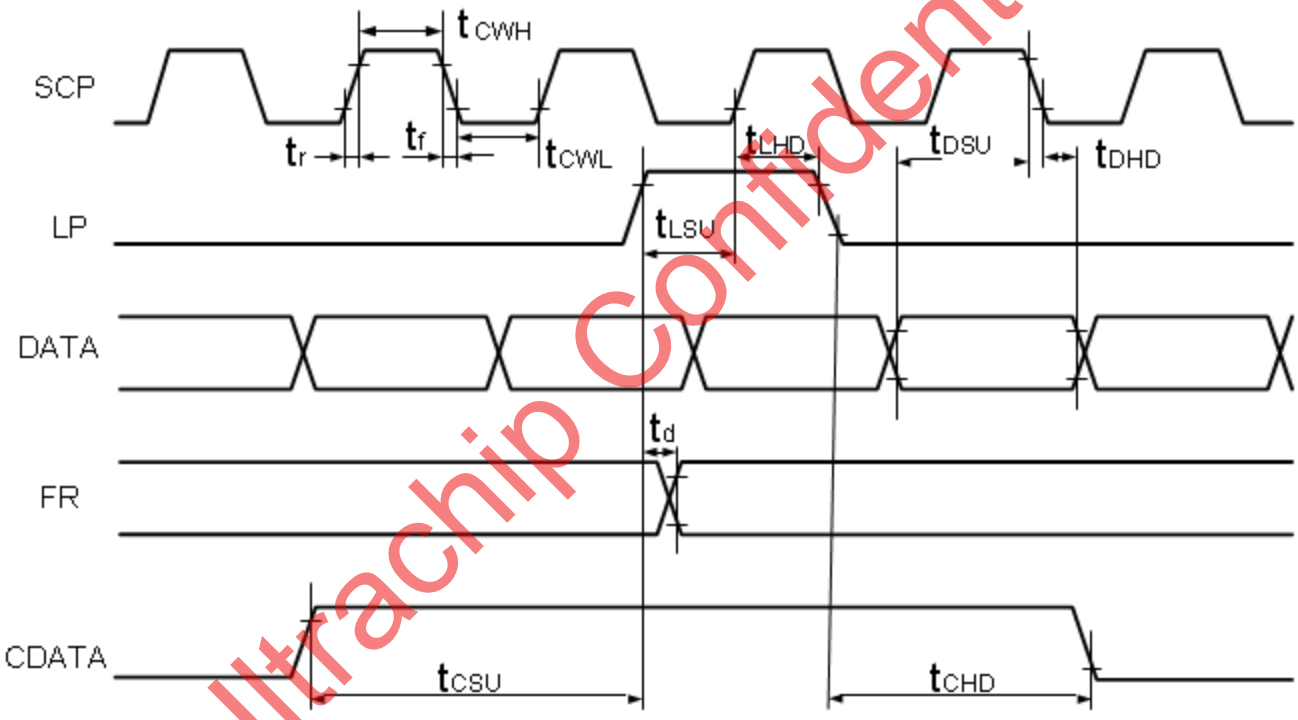
MPU Interface Timing



V_{DD} = +5V ± 5%, GND = 0V, T_A = –20~+70°C

Symbol	Item	Test Conditions	Min.	Max.	Unit
t_{CDS}	C/D Set up time		100	–-	nS
t_{CDH}	C/D Hold time		10	–-	nS
t_{CE}, t_{RD}, t_{WR}	CE , RD , WR pulse width		80	–-	nS
t_{DS}	Data set up time		80	–-	nS
t_{DH}	Data hold time		40	–-	nS
t_{ACC}	Access time		–-	150	nS
t_{OH}	Output hold time		10	50	nS

Driver Interface Timing

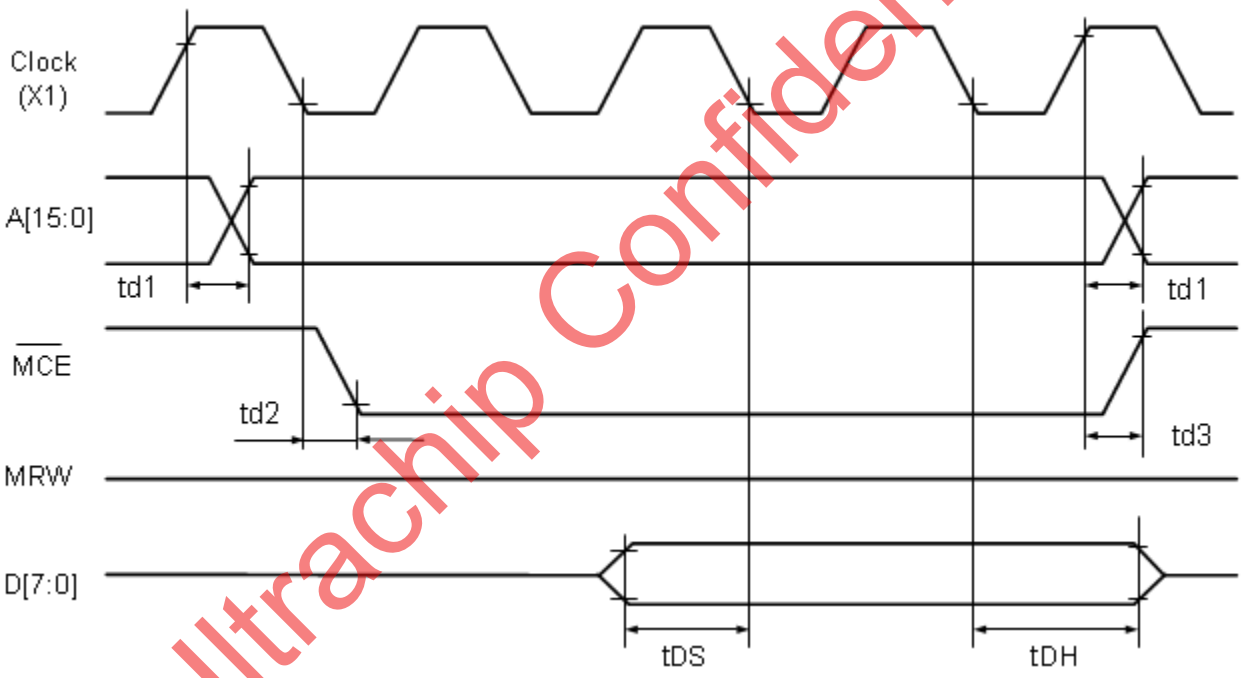


V_{DD} = +5V ± 5%, GND = 0V, T_A = –20~+70°C

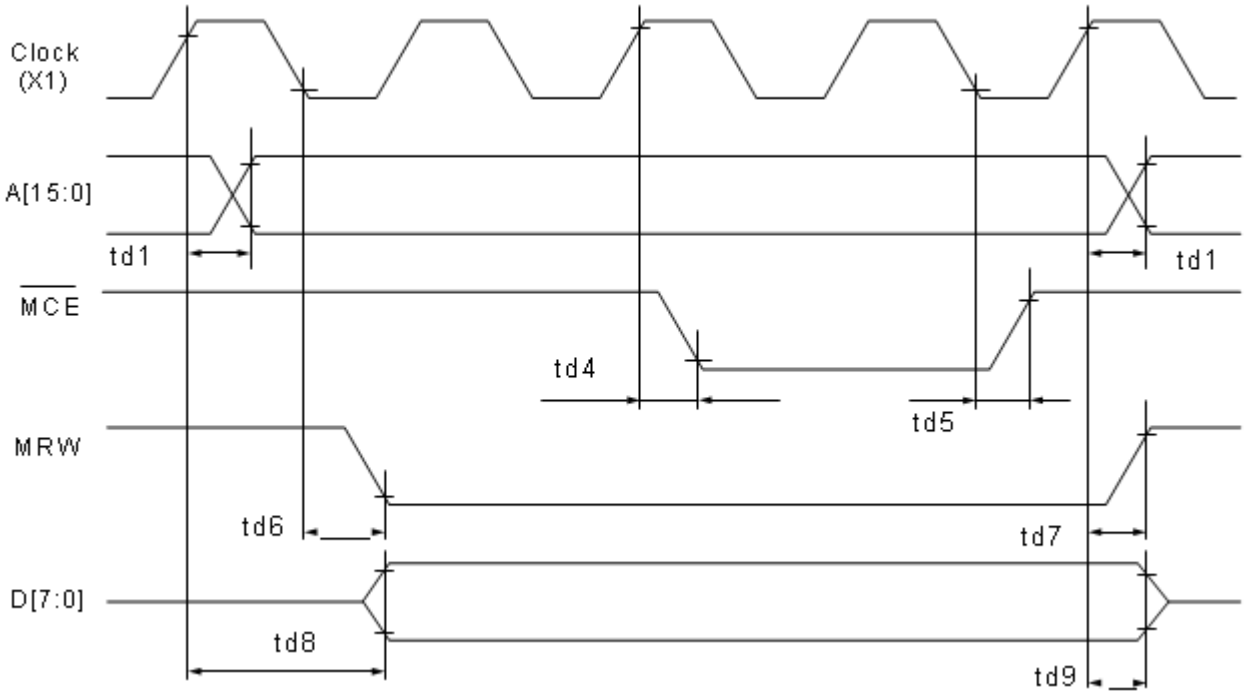
Symbol	Item	Test Conditions	Min.	Max.	Unit
f_{SCP}	Operating Frequency		–-	9	MHz
t_{CWH}, t_{CWL}	SCP pulse width		150	–-	nS
t_R, t_F	SCP rise/fall time		–-	30	nS
t_{LSU}	LP setup time		150	290	nS
t_{LHD}	LP hold time		5	40	nS
t_{DSU}	Data setup time		170	–-	nS
t_{DHD}	Data hold time		80	–-	nS
t_D	FR delay time		0	90	nS
t_{CSU}	CDATA setup time		450	850	nS
t_{CHD}	CDATA hold time		450	950	nS

External Memory Interface

External RAM –- Read



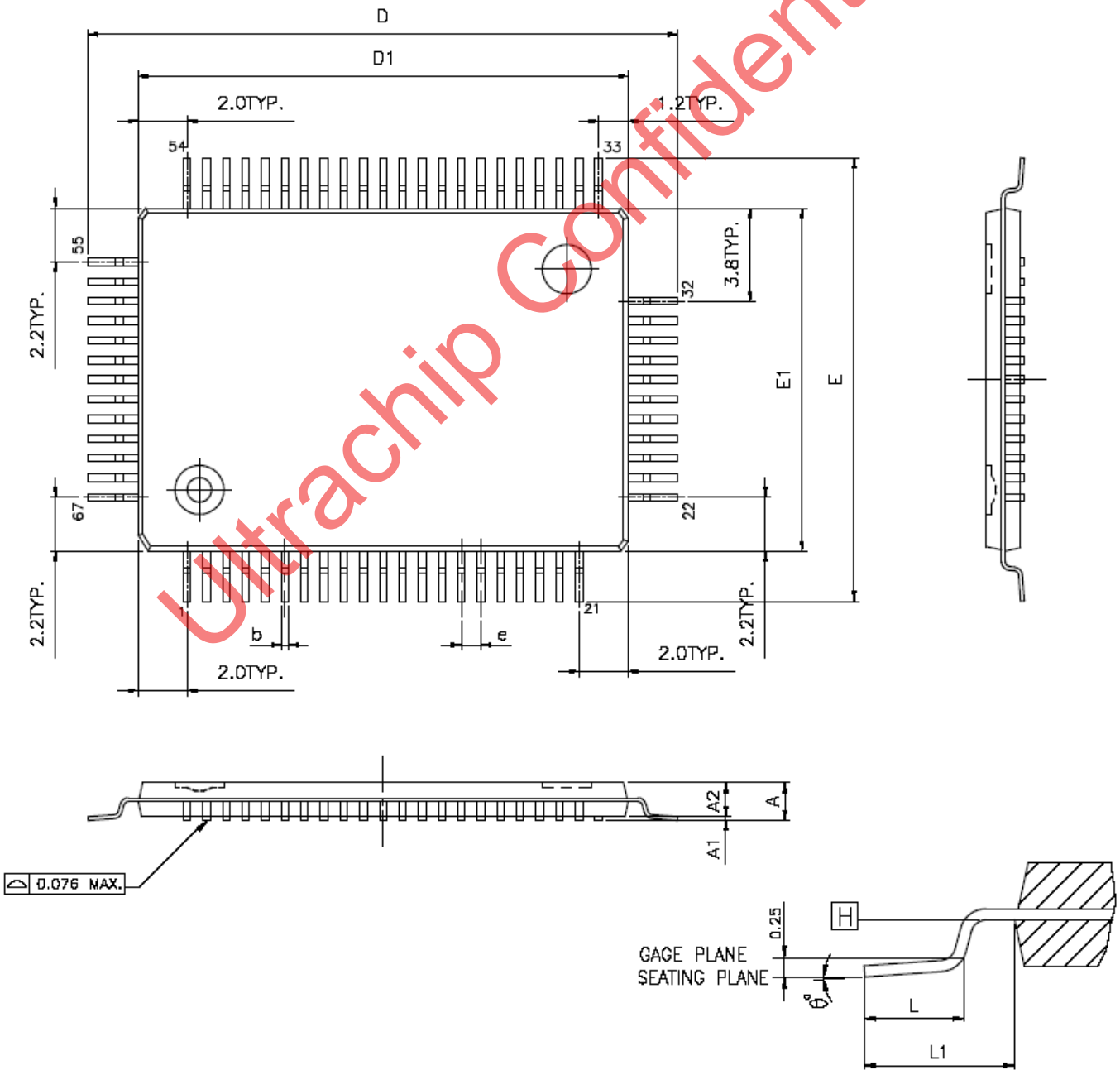
External RAM –- Write



V_{DD} = +5V ± 5%, GND = 0V, T_A = –20~+70°C

Symbol	Item	Test Conditions	Min.	Max.	Unit
f_{d1}	Address delay time		-–	250	nS
t_{d2}	$\overline{MCE}$ fall delay time (read)		–-	180	nS
t_{d3}	$\overline{MCE}$ rise delay time (read)		–-	180	nS
t_{DS}	Data setup time		0	–-	nS
t_{DH}	Data hole time		30	-–	nS
t_{d4}	$\overline{MCE}$ fall delay time (write)		–-	200	nS
t_{d5}	$\overline{MCE}$ rise delay time (write)		–-	200	nS
t_{d6}	MRW fall delay time		–-	180	nS
t_{d7}	MRW rise delay time		–-	180	nS
t_{d8}	Data stable time		–-	450	nS
t_{d9}	Data hold time		–-	200	nS

PACKAGE INFORMATION



Symbol	Min. (mm)	Nom. (mm)	Max. (mm)
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.20	0.30	0.40
D		24.10 Basic	
D1		20.00 Basic	

Symbol	Min. (mm)	Nom. (mm)	Max. (mm)
E		18.10 Basic	
E1		14.00 Basic	
e		0.8 Basic	
L	1.15	1.35	1.55
L1		2.05 Ref.	
Θ°	0	3.5	7

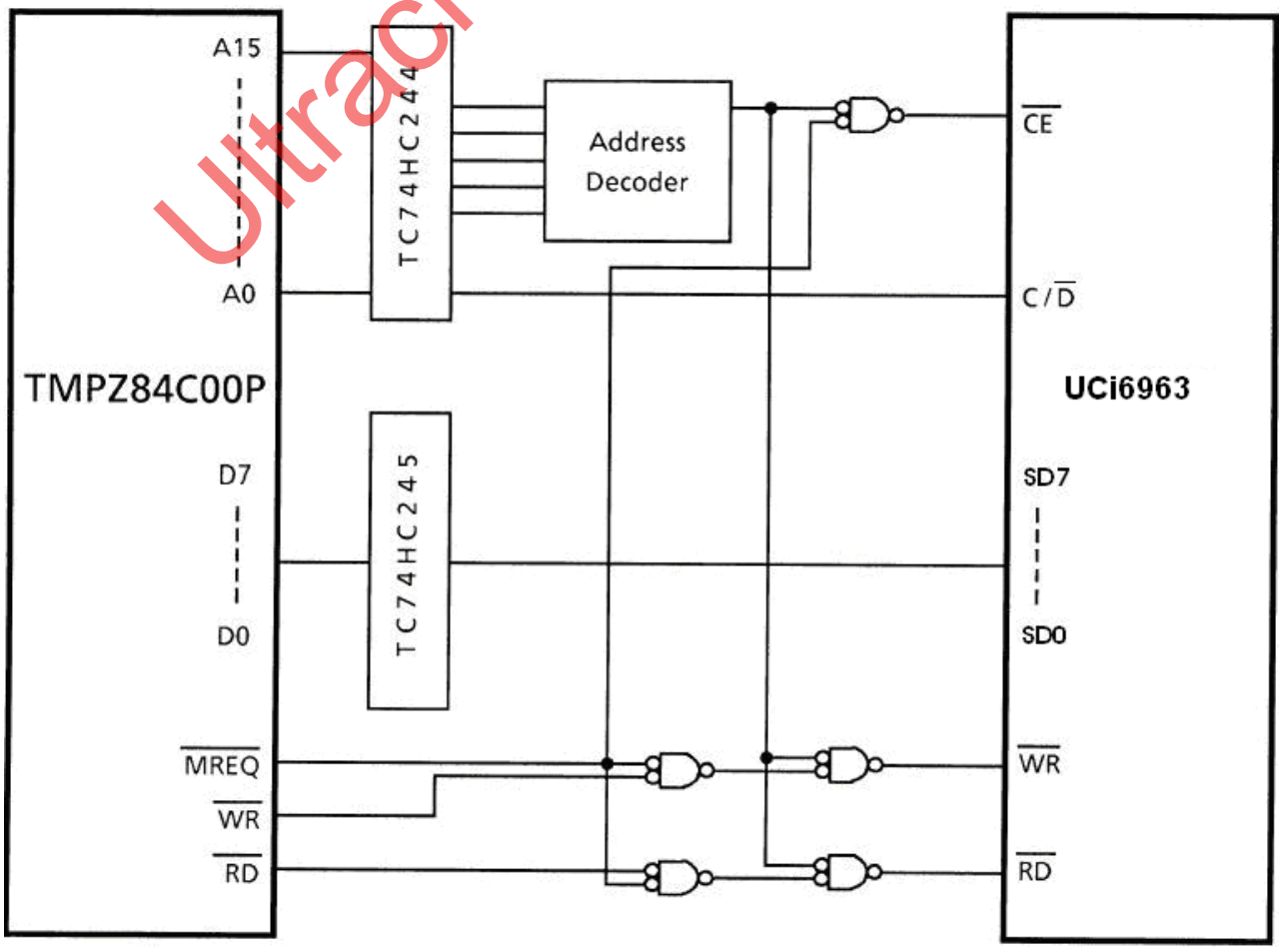
APPLICATIONS

The UCi6963 can be directly connected to Z80 (See the Note below) series MPU. The following applications are useing a TMPZ84C00A to connect UCi6963.

MPU Memory Address Mapping

Data is transferred to the UCi6963 using a memory request signal.

	Address
Data (I/O)	XXXXh
Command/Status	XXXX+1h

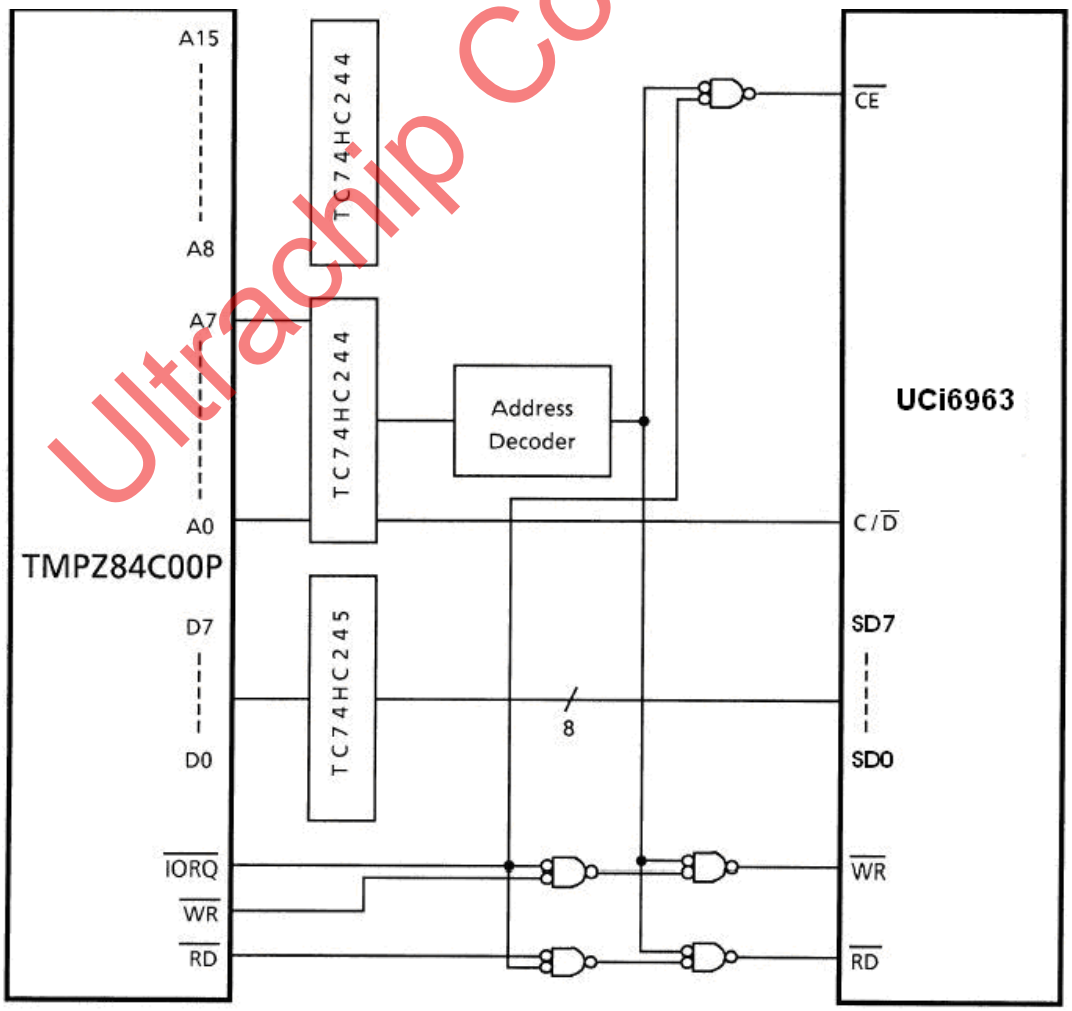


Note: Z80 is a trademark of Zilog Inc.

MPU I/O Addressing

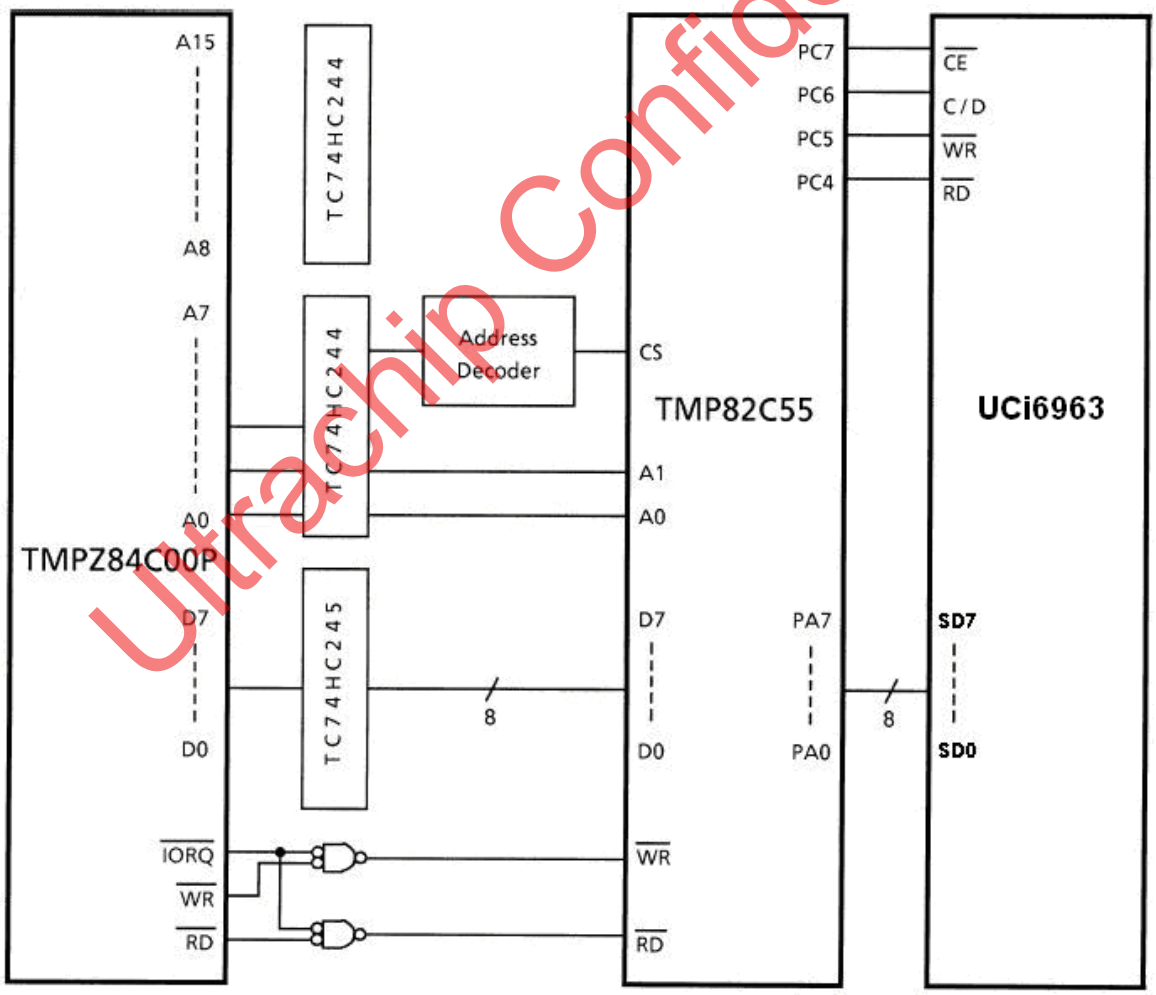
Data is transferred to the UCi6963 using an I/O request signal.

	Address
Data (I/O)	XXh
Command/Status	XX+1h



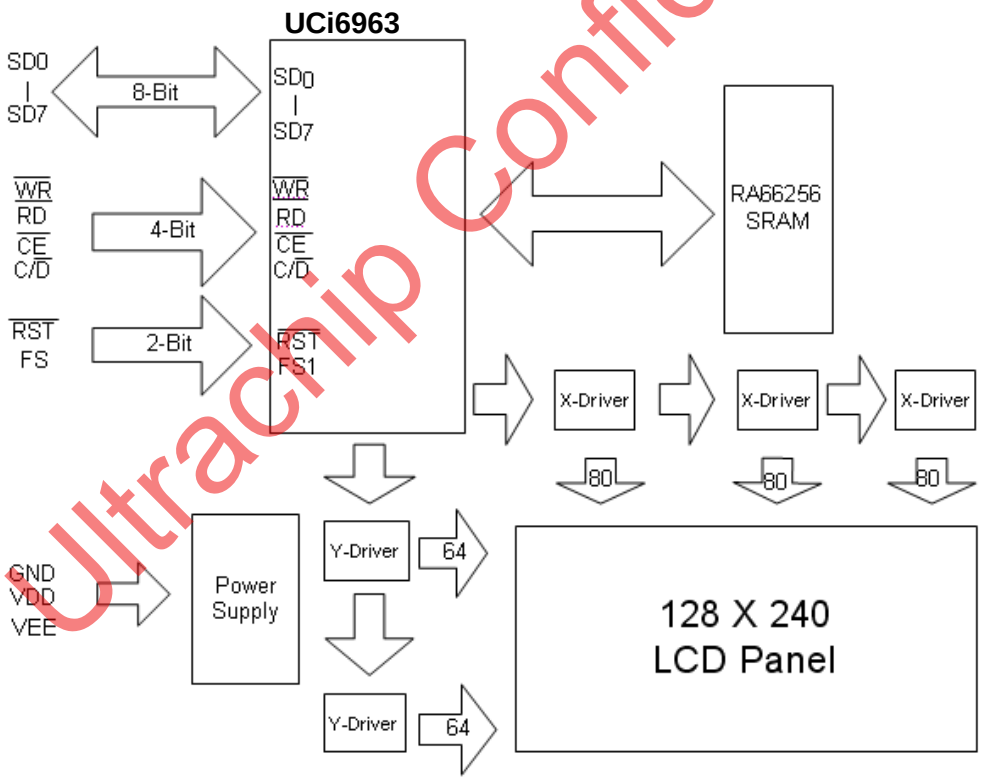
Use PPI LSI

The UCi6963 can be connected to a PPI LSI, with Port A connects to the data bus and Port C connects to the control bus (C/$\overline{D}$, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$), as shown below:

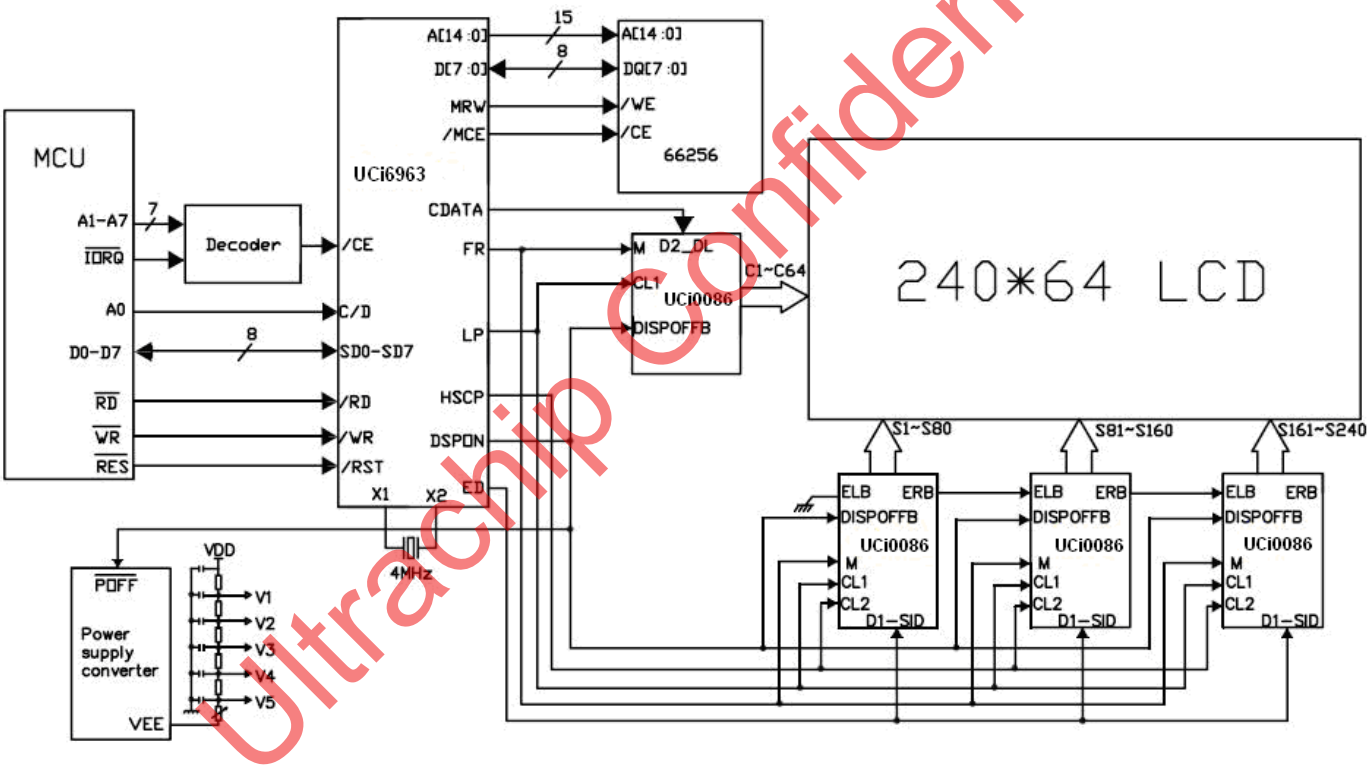


Application Block Diagram

All LCD require two power sources, VDD for logic circuits and VEE for Liquid Crystal (LC) drive. Some graphics LCD modules will run directly of a single VDD supply by generating the VEE voltage on-board; others will require an external DC-DC converter to generate the negative VEE voltage. Refer to individual specifications for details.



Application Circuit



REVISION HISTORY

Revision	Contents	Date
0.6	First Release	Sep. 30, 2011
0.61	(1) A legacy in a drawing is corrected.	Oct. 4, 2011
0.62	(1) Part Number in the Ordering Information section is updated. (2) Bare Die related sections are removed.	Mar. 15, 2012
0.63	The Pin location drawing is refined.	Jul. 10, 2012
0.7	A new section, Flowchart of Communications w/ MPU, is inserted between Control Register and Command Table.	Jun. 19, 2014