SSD1311

Advance Information

100 x 32
OLED/PLED Segment/Common Driver with Controller
For 20x4 Characters

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD1311 Specification

Version	Change Items	Effective Date
0.10	1st Release	28-Sep-10
1.0	Change to Advance info	21-Jan-11

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1311 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display. It consists of 100 segments and 32 commons while it can display 1, 2, 3, or 4 lines with 5x8 or 6x8 dots format. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1311 displays character directly from its internal 10,240 bits (256 characters x 5 x 8 dots) Character Generator ROM (CGROM). All the character codes are stored in the 640 bits (80 characters) Data Display RAM (DDRAM). User defined character can be loaded via 512 bits (8 characters) Character Generator RAM (CGRAM). Data/ Commands are sent from general MCU through software selectable 4 / 8-bit 6800/8000 series compatible Parallel Interface, I^2C interface or Serial Peripheral Interfaces.

The contrast control and oscillator which embedded in SSD1311 reduce the number of external components. With the special design on minimizing power consumption, SSD1311 is suitable for portable applications requiring a compact size.

2 FEATURES

- Resolution: 100 x 32 dot matrix panel
- Power supply (2 options selected by software command):
  [Low voltage I/O application]
  - V_{DDIO} = 2.4V to 3.6V
    (MCU interface logic level)
  - V_{DD} = 2.4V to V_{DDIO}
    (Low voltage power supply)
  - V_{CC} = 8.0V to 15.0V
    (Panel driving power supply)

  [5V I/O application]
  - V_{DDIO} = 4.4V to 5.5
    (MCU interface logic level)
  - V_{DD} is internally regulated, a stabilizing capacitor is needed
  - V_{CC} = 8.0V to 15.0V
    (Panel driving power supply)
- Segment maximum source current: 450uA
- Common maximum sink current: 45mA
- 256-step Contrast Control
- Pin selectable MCU Interfaces:
  - 4 / 8-bit 6800/8080-series parallel interface
  - Serial Peripheral Interface
  - I^2C Interface (Up to 400kbit/s)
- On-Chip Memories
  - Character Generator ROM (CGROM): 10,240 bits (256 characters x 5 x 8 dot)
  - Character Generator RAM (CGRAM): 64 x 8 bits (8 characters)
  - Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Selectable duty cycle: 1/8, 1/16, 1/24, 1/32
- 1, 2, 3 or 4 lines with 5x8 or 6x8 dots format display
- 3 sets of CGROM (ROM A / B / C – software or hardware pin selectable)
- Row Re-mapping and Column Re-mapping
- Double-height Font characters
- Bi-direction shift function
- All character reverse display
- Display shift per line
- Automatic power on reset
- Screen saving continuous scrolling function in horizontal direction (character by character)
- Screen saving fade in / out feature
- Programmable Frame Frequency
- Smart Cross-talk compensation scheme
- On-Chip Oscillator
- Chip layout for COG
- Wide range of operating temperatures:
  -40°C to 85°C

2.1 5-dot / 6-dot font width

Table 2-1: 5-dot / 6-dot font width

Display Line Numbers	Duty Ratio	5-dot font width	6-dot font width
		Displayable Characters	Displayable Characters
1	1/8	1 line of 20 characters	1 line of 16 characters
2	1/16	2 lines of 20 characters	2 lines of 16 characters
3	1/24	3 lines of 20 characters	3 lines of 16 characters
4	1/32	4 lines of 20 characters	4 lines of 16 characters

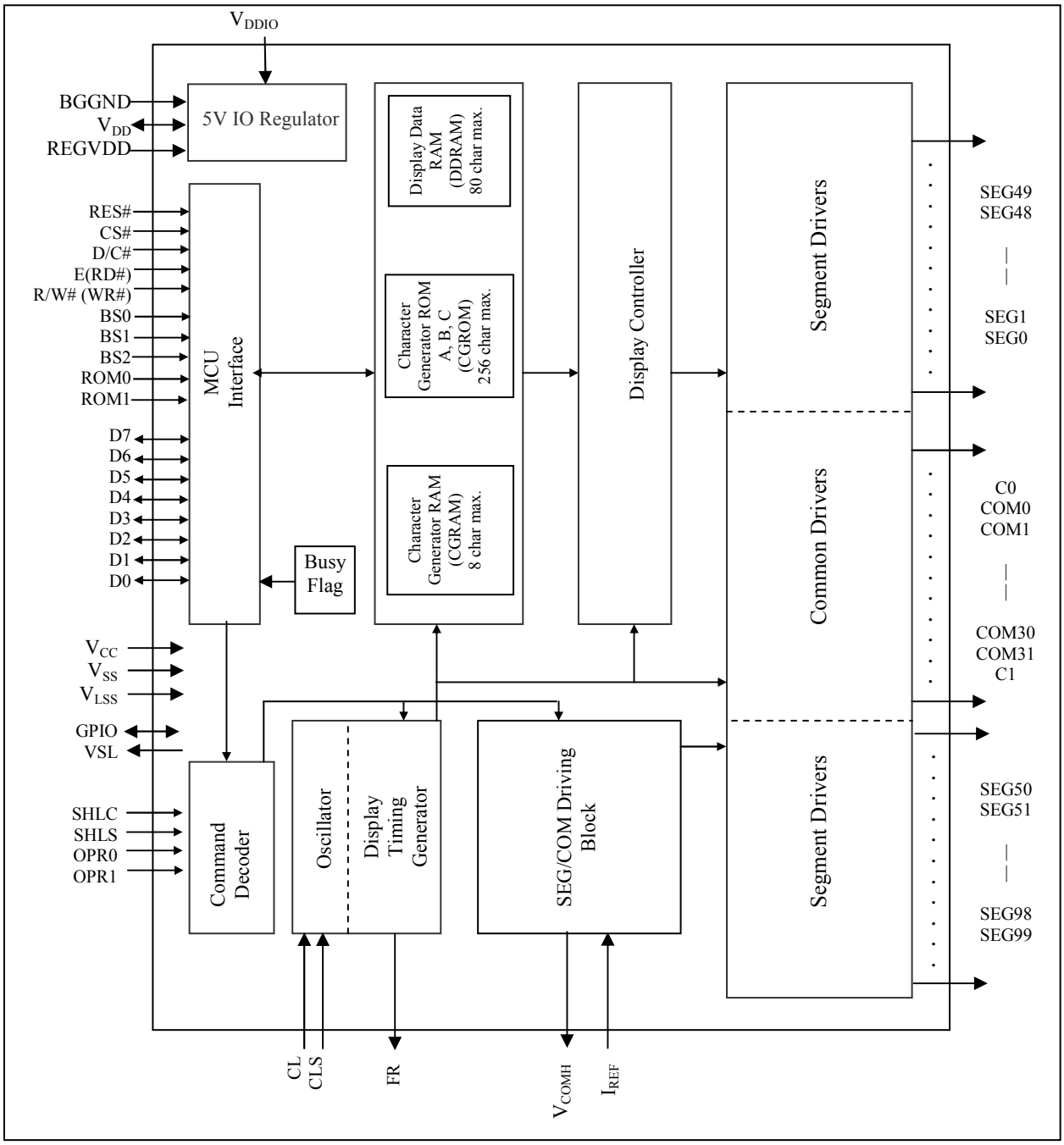
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	CGROM	Package Form	Reference	Remark
SSD1311M1Z	100	32	A, B, C	COG	Page 10, 65	○ Min SEG pad pitch : 37.6 um ○ Min COM pad pitch : 40 um ○ Min I/O pad pitch : 60 um ○ Die thickness: 300 +/- 15um ○ Bump height: nominal 12um

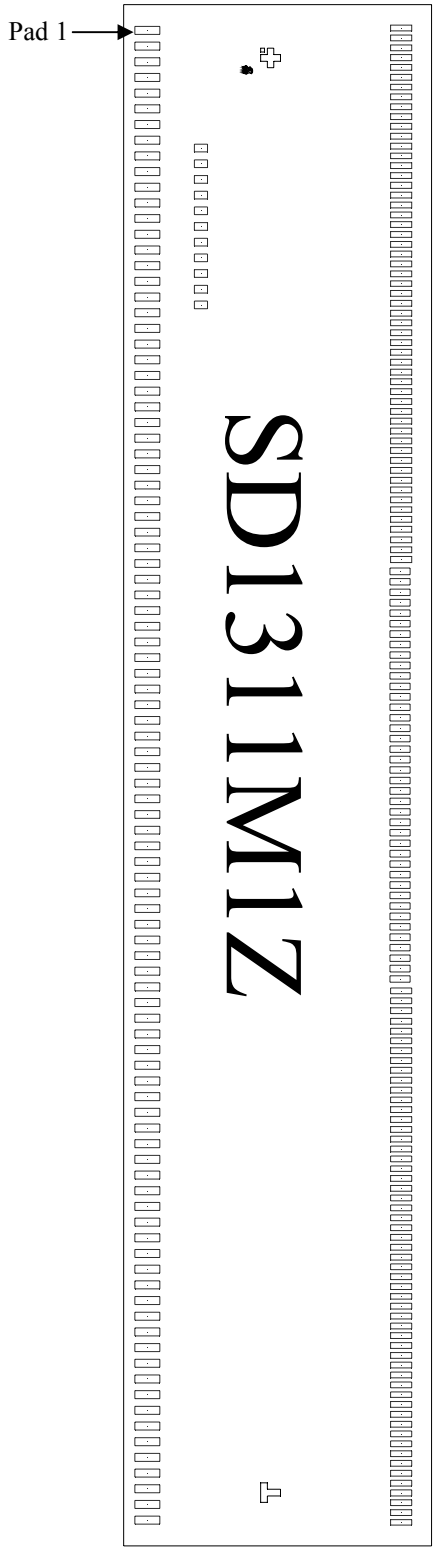
4 BLOCK DIAGRAM

Figure 4-1: SSD1311 Block Diagram



5 DIE PAD FLOOR PLAN

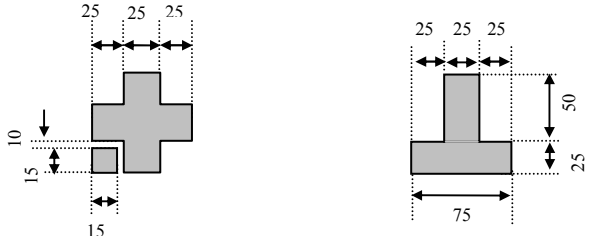
Figure 5-1 – SSD1311Z Die Drawing



Die size (after sawing)	5.9 ± 0.05mm x 1.2 ± 0.05mm
Die thickness	300 +/- 15um
Min I/O pad pitch	60 um
Min SEG pad pitch	37.6um
Min COM pad pitch	40 um
Bump height	Nominal 12 um

Bump Size		
Pad #	X [um]	Y [um]
1~96	30	95
97~151 192~246	22	80
152~191	25	77
247~257	30	50

Alignment mark	Position	Size
T shape	(2745, -27)	75um x 75um
+ shape	(-2745, -27)	75um x 75um



Note

(1) Diagram showing the Gold bumps face up.
(2) Coordinates are referenced to center of the chip.
(3) Coordinate units and size of all alignment marks are in um.
(4) All alignment keys do not contain gold.

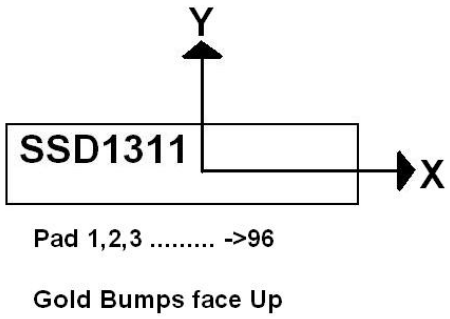


Table 5-1 : SSD1311 Bump Die Pad Coordinates

Pin number	Pin name	X	Y
1	NC	-2850	-495
2	NC	-2790	-495
3	NC	-2730	-495
4	NC	-2670	-495
5	NC	-2610	-495
6	VSL	-2550	-495
7	VSL	-2490	-495
8	VLSS	-2430	-495
9	VLSS	-2370	-495
10	VLSS	-2310	-495
11	NC	-2250	-495
12	VCC	-2190	-495
13	VCC	-2130	-495
14	VCC	-2070	-495
15	VCC	-2010	-495
16	VCOMH	-1950	-495
17	VCOMH	-1890	-495
18	VCOMH	-1830	-495
19	VCOMH	-1770	-495
20	NC	-1710	-495
21	VLSS	-1650	-495
22	VLSS	-1590	-495
23	VSS	-1530	-495
24	VSS	-1470	-495
25	VSS	-1410	-495
26	BGGND	-1350	-495
27	VSS	-1290	-495
28	REGVDD	-1230	-495
29	VDDIO	-1170	-495
30	SHLC	-1110	-495
31	VSS	-1050	-495
32	SHLS	-990	-495
33	VDDIO	-930	-495
34	VDD	-870	-495
35	VDD	-810	-495
36	VDDIO	-750	-495
37	VDDIO	-690	-495
38	VDDIO	-630	-495
39	BS0	-570	-495
40	VSS	-510	-495
41	BS1	-450	-495
42	VDDIO	-390	-495
43	BS2	-330	-495
44	VSS	-270	-495
45	GPIO	-210	-495
46	FR	-150	-495
47	CL	-90	-495
48	VSS	-30	-495
49	CS#	30	-495
50	RES#	90	-495
51	D/C#	150	-495
52	VSS	210	-495
53	R/W#(WR#)	270	-495
54	E(RD#)	330	-495
55	D0	390	-495
56	D1	450	-495
57	D2	510	-495
58	D3	570	-495
59	VSS	630	-495
60	D4	690	-495
61	D5	750	-495
62	D6	810	-495
63	D7	870	-495
64	IREF	930	-495
65	VSS	990	-495
66	CLS	1050	-495
67	VDDIO	1110	-495
68	ROM0	1170	-495
69	VSS	1230	-495
70	ROM1	1290	-495
71	VDDIO	1350	-495
72	OPR0	1410	-495
73	VSS	1470	-495
74	OPR1	1530	-495
75	VDDIO	1590	-495
76	VDDIO	1650	-495
77	VDD	1710	-495
78	VDD	1770	-495
79	VCOMH	1830	-495
80	VCOMH	1890	-495
81	VCOMH	1950	-495
82	VCOMH	2010	-495
83	VCC	2070	-495
84	VCC	2130	-495
85	VCC	2190	-495
86	VCC	2250	-495
87	VCC	2310	-495
88	NC	2370	-495
89	VLSS	2430	-495
90	VLSS	2490	-495
91	VLSS	2550	-495
92	NC	2610	-495
93	NC	2670	-495
94	NC	2730	-495
95	NC	2790	-495
96	NC	2850	-495
97	VCC	2858.85	469
98	VCC	2821.25	469
99	SEG49	2783.65	469
100	SEG48	2746.05	469
101	SEG47	2708.45	469
102	SEG46	2670.85	469
103	SEG45	2633.25	469
104	SEG44	2595.65	469
105	SEG43	2558.05	469
106	SEG42	2520.45	469
107	SEG41	2482.85	469
108	SEG40	2445.25	469
109	SEG39	2407.65	469
110	SEG38	2370.05	469
111	SEG37	2332.45	469
112	SEG36	2294.85	469
113	SEG35	2257.25	469
114	SEG34	2219.65	469
115	SEG33	2182.05	469
116	SEG32	2144.45	469
117	SEG31	2106.85	469
118	SEG30	2069.25	469
119	SEG29	2031.65	469
120	SEG28	1994.05	469
121	SEG27	1956.45	469
122	SEG26	1918.85	469
123	SEG25	1881.25	469
124	SEG24	1843.65	469
125	SEG23	1806.05	469
126	SEG22	1768.45	469
127	SEG21	1730.85	469
128	SEG20	1693.25	469
129	SEG19	1655.65	469
130	SEG18	1618.05	469
131	SEG17	1580.45	469
132	SEG16	1542.85	469
133	SEG15	1505.25	469
134	SEG14	1467.65	469
135	SEG13	1430.05	469
136	SEG12	1392.45	469
137	SEG11	1354.85	469
138	SEG10	1317.25	469
139	SEG9	1279.65	469
140	SEG8	1242.05	469
141	SEG7	1204.45	469
142	SEG6	1166.85	469
143	SEG5	1129.25	469
144	SEG4	1091.65	469
145	SEG3	1054.05	469
146	SEG2	1016.45	469
147	SEG1	978.85	469
148	SEG0	941.25	469
149	VCC	900.62	469
150	VCC	863.02	469
151	VCC	825.42	469
152	VCOMH	780	464.5
153	VCOMH	740	464.5
154	VCOMH	700	464.5
155	C0	660	464.5
156	COM0	620	464.5
157	COM1	580	464.5
158	COM2	540	464.5
159	COM3	500	464.5
160	COM4	460	464.5
161	COM5	420	464.5
162	COM6	380	464.5
163	COM7	340	464.5
164	COM8	300	464.5
165	COM9	260	464.5
166	COM10	220	464.5
167	COM11	180	464.5
168	COM12	140	464.5
169	COM13	100	464.5
170	COM14	60	464.5
171	COM15	20	464.5
172	COM16	-20	464.5
173	COM17	-60	464.5
174	COM18	-100	464.5
175	COM19	-140	464.5
176	COM20	-180	464.5
177	COM21	-220	464.5
178	COM22	-260	464.5
179	COM23	-300	464.5
180	COM24	-340	464.5
181	COM25	-380	464.5
182	COM26	-420	464.5
183	COM27	-460	464.5
184	COM28	-500	464.5
185	COM29	-540	464.5
186	COM30	-580	464.5
187	COM31	-620	464.5
188	C1	-660	464.5
189	VCOMH	-700	464.5
190	VCOMH	-740	464.5
191	VCOMH	-780	464.5
192	VCC	-825.42	469
193	VCC	-863.02	469
194	VCC	-900.62	469
195	SEG50	-941.25	469
196	SEG51	-978.85	469
197	SEG52	-1016.45	469
198	SEG53	-1054.05	469
199	SEG54	-1091.65	469
200	SEG55	-1129.25	469
201	SEG56	-1166.85	469
202	SEG57	-1204.45	469
203	SEG58	-1242.05	469
204	SEG59	-1279.65	469
205	SEG60	-1317.25	469
206	SEG61	-1354.85	469
207	SEG62	-1392.45	469
208	SEG63	-1430.05	469
209	SEG64	-1467.65	469
210	SEG65	-1505.25	469
211	SEG66	-1542.85	469
212	SEG67	-1580.45	469
213	SEG68	-1618.05	469
214	SEG69	-1655.65	469
215	SEG70	-1693.25	469
216	SEG71	-1730.85	469
217	SEG72	-1768.45	469
218	SEG73	-1806.05	469
219	SEG74	-1843.65	469
220	SEG75	-1881.25	469
221	SEG76	-1918.85	469
222	SEG77	-1956.45	469
223	SEG78	-1994.05	469
224	SEG79	-2031.65	469
225	SEG80	-2069.25	469
226	SEG81	-2106.85	469
227	SEG82	-2144.45	469
228	SEG83	-2182.05	469
229	SEG84	-2219.65	469
230	SEG85	-2257.25	469
231	SEG86	-2294.85	469
232	SEG87	-2332.45	469
233	SEG88	-2370.05	469
234	SEG89	-2407.65	469
235	SEG90	-2445.25	469
236	SEG91	-2482.85	469
237	SEG92	-2520.45	469
238	SEG93	-2558.05	469
239	SEG94	-2595.65	469
240	SEG95	-2633.25	469
241	SEG96	-2670.85	469
242	SEG97	-2708.45	469
243	SEG98	-2746.05	469
244	SEG99	-2783.65	469
245	VCC	-2821.25	469
246	VCC	-2858.85	469
247	TR9	-2399.9	-290.81
248	TR8	-2339.9	-290.81
249	TR7	-2279.9	-290.81
250	TR6	-2219.9	-290.81
251	TR5	-2159.9	-290.81
252	VSS	-2099.9	-290.81
253	TR4	-2039.9	-290.81
254	TR3	-1979.9	-290.81
255	TR2	-1919.9	-290.81
256	TR1	-1859.9	-290.81
257	TR0	-1799.9	-290.81

6 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 6-1 : SSD1311 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply for core logic operation. V_{DD} can be supplied externally or regulated internally. In LV IO application (internal V_{DD} is disabled), this is a power input pin. In 5V IO application (internal V_{DD} is enabled), V_{DD} is regulated internally from V_{DDIO}. A capacitor should be connected between V_{DD} and V_{SS} under all circumstances.
V_{DDIO}	P	Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}. No external power supply is allowed to connect to this pin.
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain current of around 15uA.
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. **Table 6-2 : Bus Interface selection** BS[2:0] / Interface 000 / Serial Interface 001 / Invalid 010 / I^2C 011 / Invalid 100 / 8-bit 6800 parallel 101 / 4-bit 6800 parallel 110 / 8-bit 8080 parallel 111 / 4-bit 8080 parallel **Note** (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DDIO}

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>BGGND</td><td>P</td><td>Reserved pin. It should be connected to ground.</td></tr>
<tr><td>REGVDD</td><td>I</td><td>Internal V_{DD} regulator selection pin in 5V I/O application mode.

When this pin is pulled HIGH, internal V_{DD} regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal V_{DD} regulator is disabled (Low voltage I/O application).

Under 5V I/O application mode, internal V_{DD} regulator can also be disabled by extended command 71h “Function Selection A” for power saving; details refer to Table 8-2.</td></tr>
<tr><td>SHLC</td><td>I</td><td>This pin is used to determine the Common output scanning direction.

Table 6-3 : COM scan direction
<table><tr><td>SHLC</td><td>COM scan direction</td></tr><tr><td>1</td><td>COM0 to COM31 (Normal)</td></tr><tr><td>0</td><td>COM31 to COM0 (Reverse)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>SHLS</td><td>I</td><td>This pin is used to change the mapping between the display data column address and the Segment driver. Refer to Section Table 8-4 for details.

Table 6-4 : SEG scan direction
<table><tr><td>SHLS</td><td>SEG direction</td></tr><tr><td>1</td><td>SEG0 to SEG99 (Normal)</td></tr><tr><td>0</td><td>SEG99 to SEG0 (Reverse)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>ROM[1:0]</td><td>I</td><td>These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table:

Table 6-5 : Character ROM selection
<table><tr><td>ROM1</td><td>ROM0</td><td>ROM</td></tr><tr><td>0</td><td>0</td><td>A</td></tr><tr><td>0</td><td>1</td><td>B</td></tr><tr><td>1</td><td>0</td><td>C</td></tr><tr><td>1</td><td>1</td><td>S/W selectable (3)</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}
(3) S/W selectable by extended command 72h “Function Selection B”; details refer to Table 8-2.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>OPR[1:0]</td><td>I</td><td>This pin is used to select the character number of character generator. Refer to Table 7-4 for details. OPR1 and OPR0 are pin select such that
Table 6-6 : Character RAM selection
<table>
<tr><td>OPR1</td><td>OPR0</td><td>CGROM</td><td>CGRAM</td></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>250</td><td>6</td></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
</table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>GPIO</td><td>I/O</td><td>It is a GPIO pin. Details refer to OLED command DCh.</td></tr>
<tr><td>VSL</td><td>P</td><td>This is segment voltage (output low level) reference pin.

When external VSL is not used, this pin should be left open.

When external VSL is used, connect with resistor and diode to ground (details depend on application).</td></tr>
<tr><td>CL</td><td>I</td><td>External clock input pin.

When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.

When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal clock selection pin.

When this pin is pulled HIGH, internal oscillator is enabled (normal operation).

When this pin is pulled LOW, an external clock signal should be connected to CL.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.

The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).

In I^2C mode, this pin must be connected to V_{SS}.</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.

When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.

In I^2C mode, this pin acts as SA0 for slave address selection.

When serial interface is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Name	Pin Type	Description
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used. Refer to Section 7.4 for details.
SEG0 ~ SEG99	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM0 ~ COM31	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
C[1:0]	-	These pins are reserved. Nothing should be connected to these pins, nor are they connected together.
TR[9:0]	-	These pins are reserved. Nothing should be connected to these pins, nor are they connected together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface selection

SSD1311 has all four kinds of interface type with MCU: I^2C, serial, 4-bit bus and 8-bit bus. Different MCU modes can be set by hardware selection on BS[2:0] pins; refer to Table 6-2 for BS[2:0] setting. This chip MCU interface consists of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1.

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
4-bit 6800	D[7:4]				Tie LOW				E	R/W#	CS#	D/C#	RES#
4-bit 8080	D[7:4]				Tie LOW				RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
Serial Interface	Tie LOW					SOD	SID	SCLK	Tie LOW		CS#	Tie LOW	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

7.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

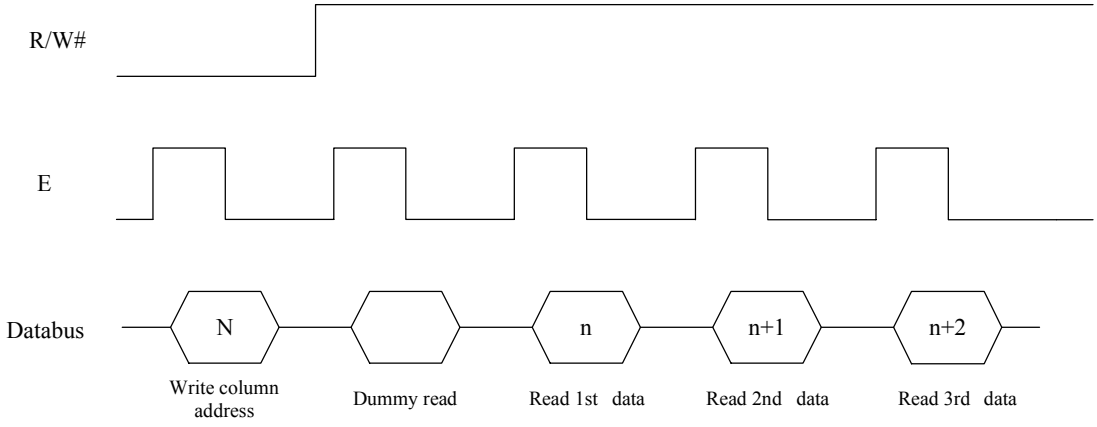
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1: Data read back procedure - insertion of dummy read



In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.
When interfacing data length is 4-bit, only 4 ports, D[7:4], are used as data bus; the unused 4 ports, D[3:0] are recommended to tie to GND.
At first higher 4-bit (in case of 8-bit bus mode, the contents of D4 - D7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of D0 - D3) are transferred. So transfer is performed by two times.

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from D[7:0].

7.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2: Example of Write procedure in 8080 parallel interface mode

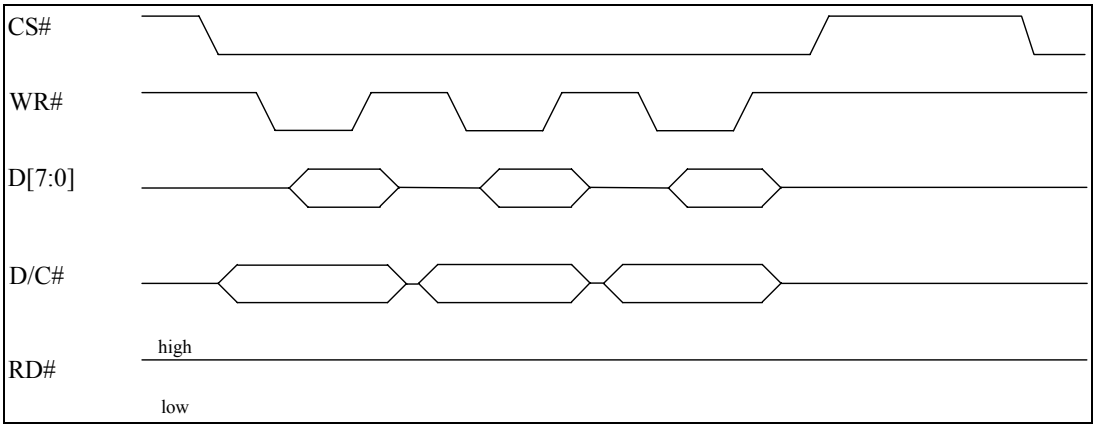


Figure 7-3: Example of Read procedure in 8080 parallel interface mode

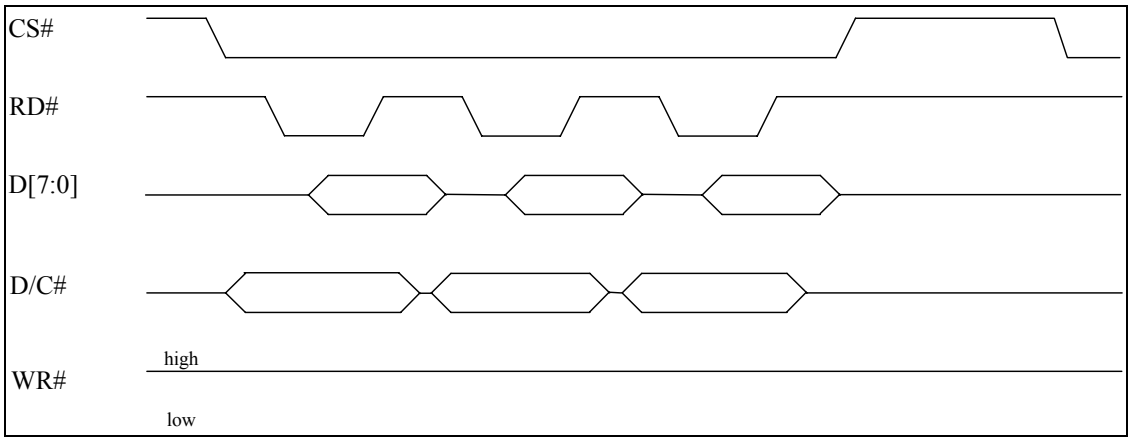


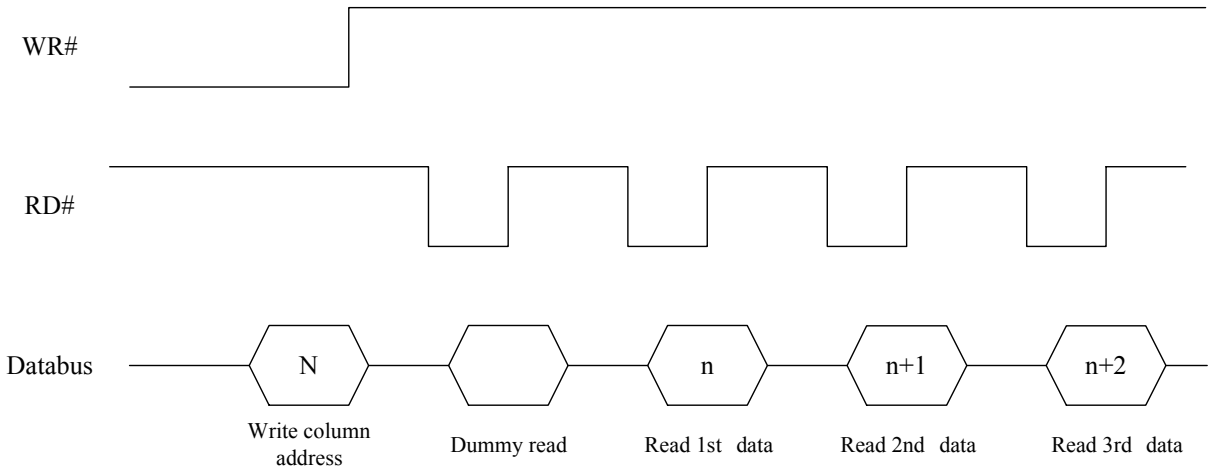
Table 7-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4: Display data read back procedure - insertion of dummy read



7.1.3 Serial Interface

When serial interface mode is started, all the three ports, SCLK (synchronizing transfer clock; i.e. D0), SID (serial input data; i.e. D1), and SOD (serial output data; i.e. D2), are used**.** If SSD1311 is used with other chips, chip select port (CS#) can be used. By setting CS# to "Low", SSD1311 can receive SCLK input. If CS# is set to "High", SSD1311 resets the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding five "High" bits, read write control bit (R/W), register selection bit (DC) and end bit that indicates the end of start byte. Whenever succeeding five "High" bits are detected by SSD1311, it makes serial transfer counter reset and ready to receive next information.

The next input data are register selection bit that determine which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to Figure 7-5 and Figure 7-6).

7.1.3.1 Write Operation (R/W = 0)

After start byte is transferred from MPU to SSD1311, 8-bit data is transferred which is divided into 2 bytes, each byte has four bit's real data and four bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where the 2nd and the 4th four bits must be "0000" for safe transfer. To transfer several bytes continuously without changing D/C bit and R/W bit, start byte transfer is needed only at first starting time. Namely, after first start byte is transferred, real data can be transferred succeeding.

7.1.3.2 Read Operation (R/W = 1)

After start byte is transferred to SSD1311, MPU can receive 8-bit data through the SOD port at a time from the LSB. Wait time is needed to insert between start byte and data reading, because internal reading from RAM requires some delay. Continuous data reading is possible like serial write operation. It also needs only one start byte, only if some delay between reading operations of each byte is inserted. During the reading operation, SSD1311 observes succeeding five "High" from MPU. If it is detected, SSD1311 restarts serial operation at once and ready to receive DC bit. So in continuous reading operation, SID port must be "Low".

Figure 7-5: Timing Diagram of Serial Data Transfer

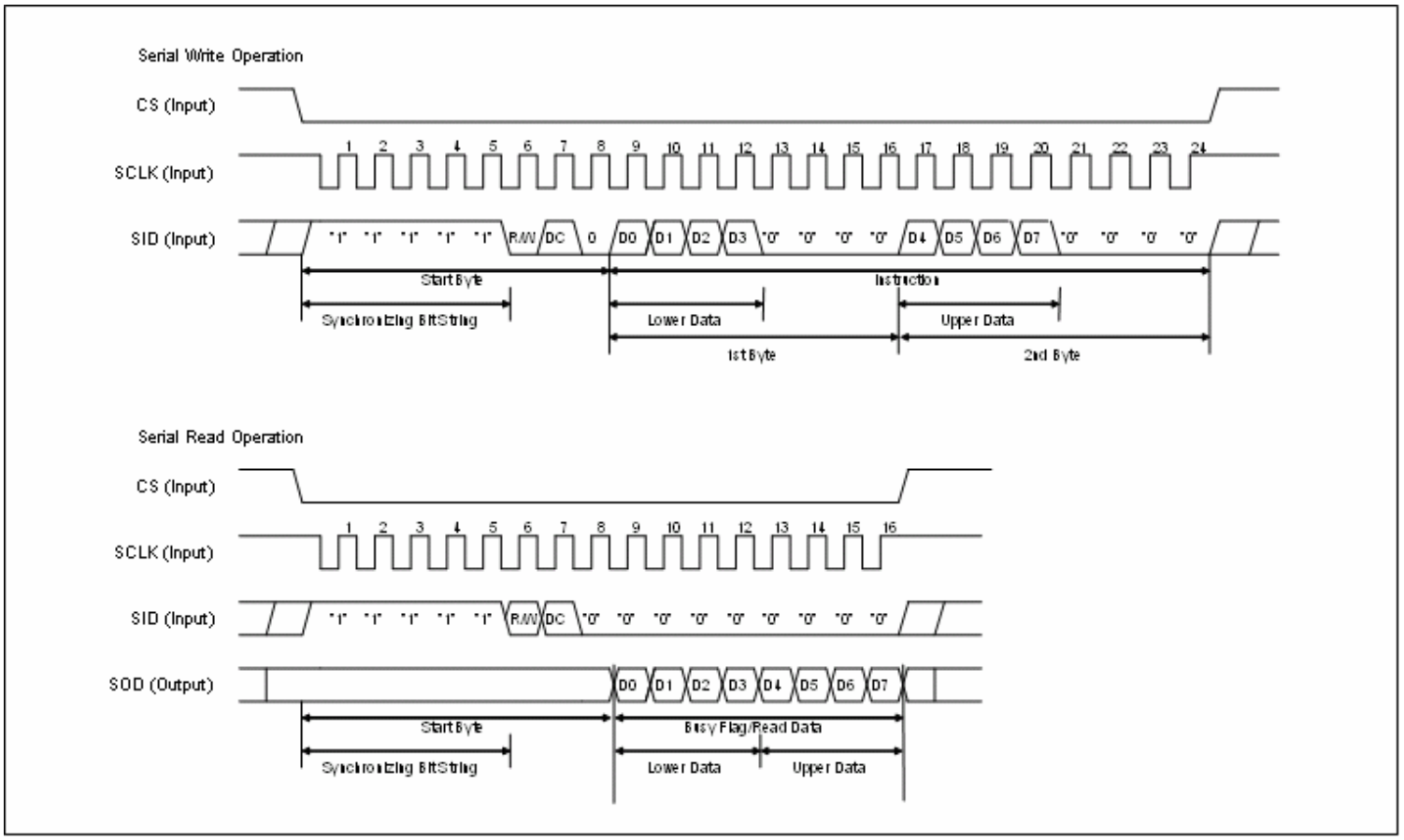
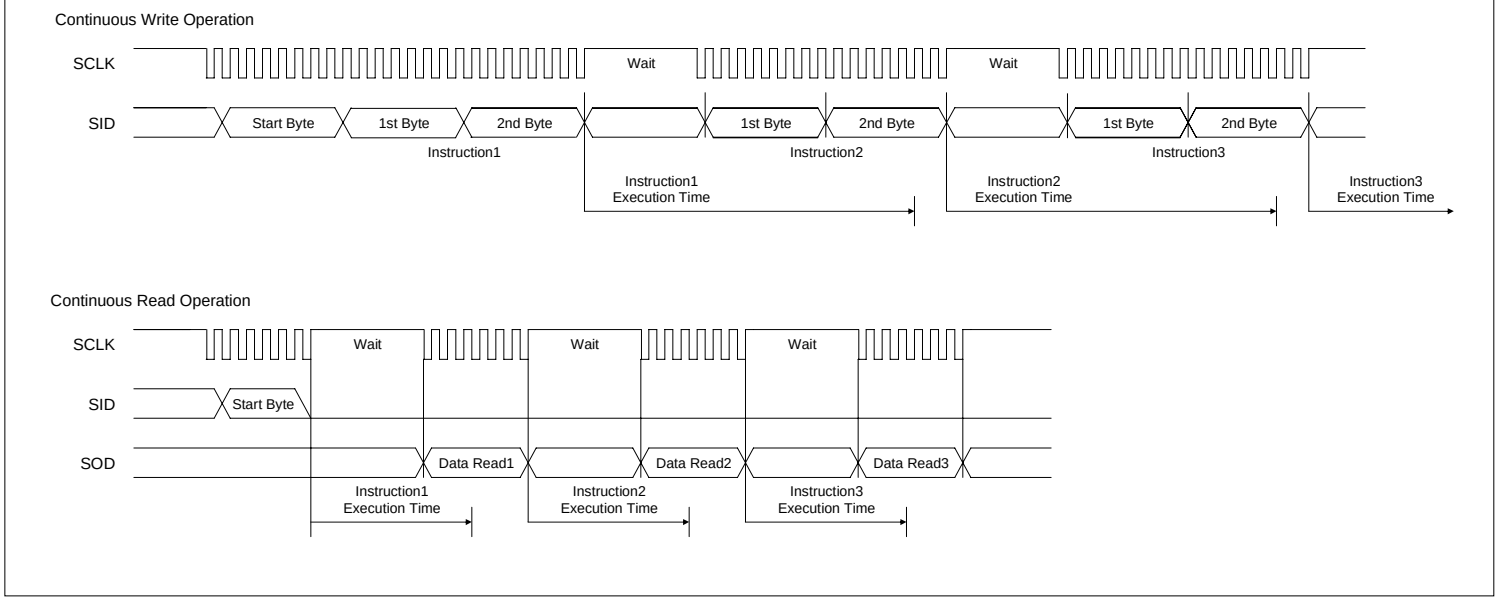


Figure 7-6: Timing Diagram of Continuous Data Transfer



7.1.4 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1311 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1311. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

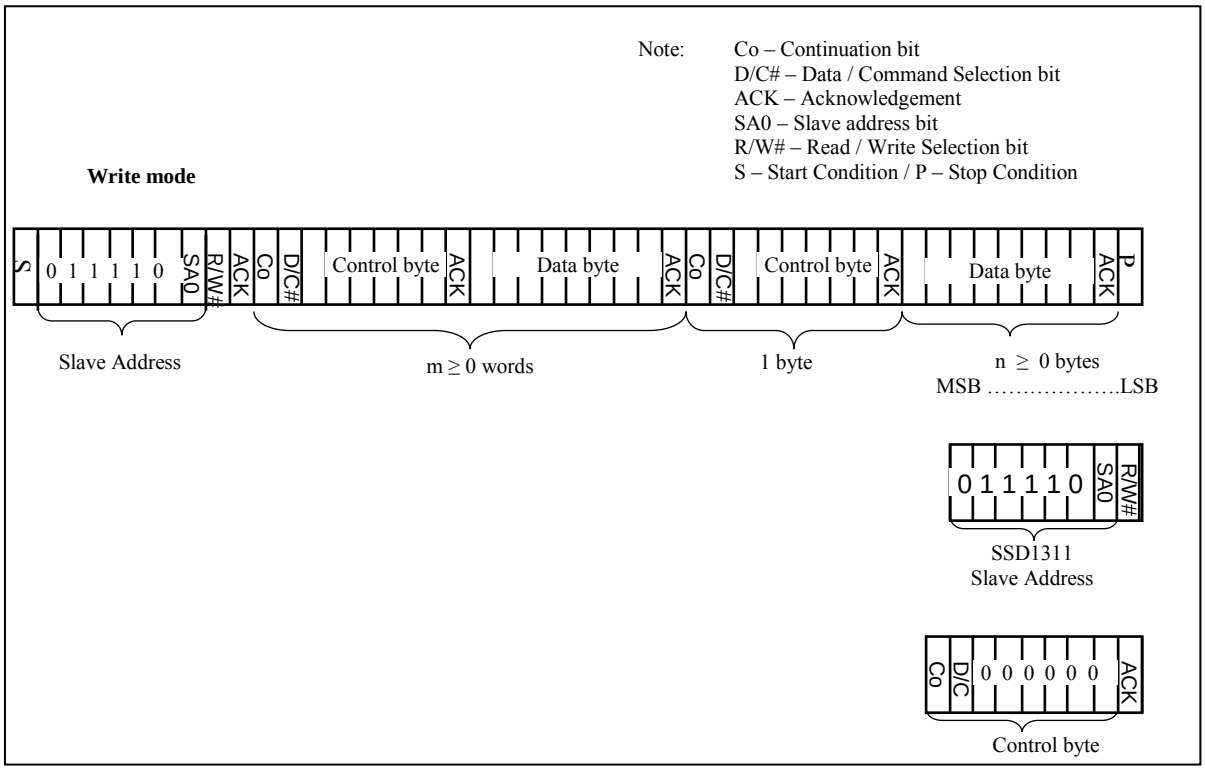
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.1.4.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-7 for the write mode of I²C-bus in chronological order.

Figure 7-7 : I²C-bus data format



7.1.4.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1311, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0"'s.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 7-8 : Definition of the Start and Stop Condition

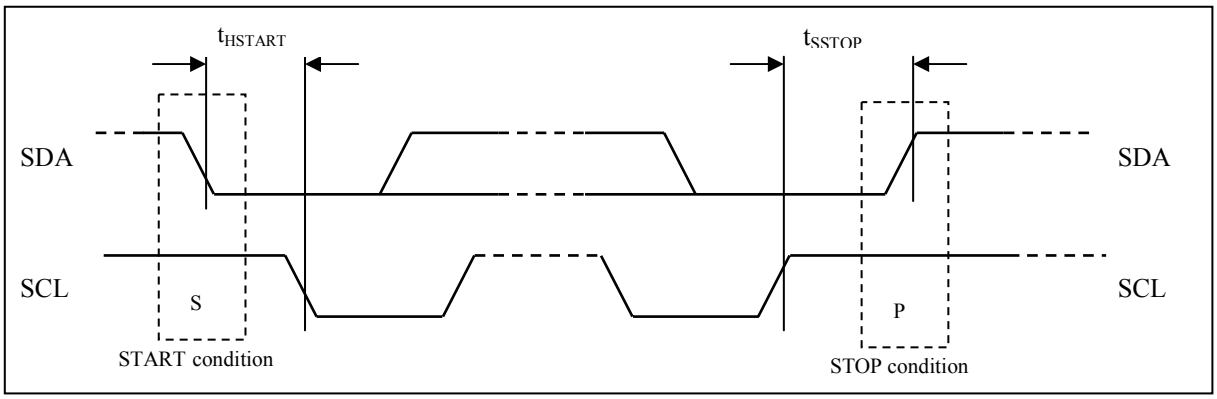
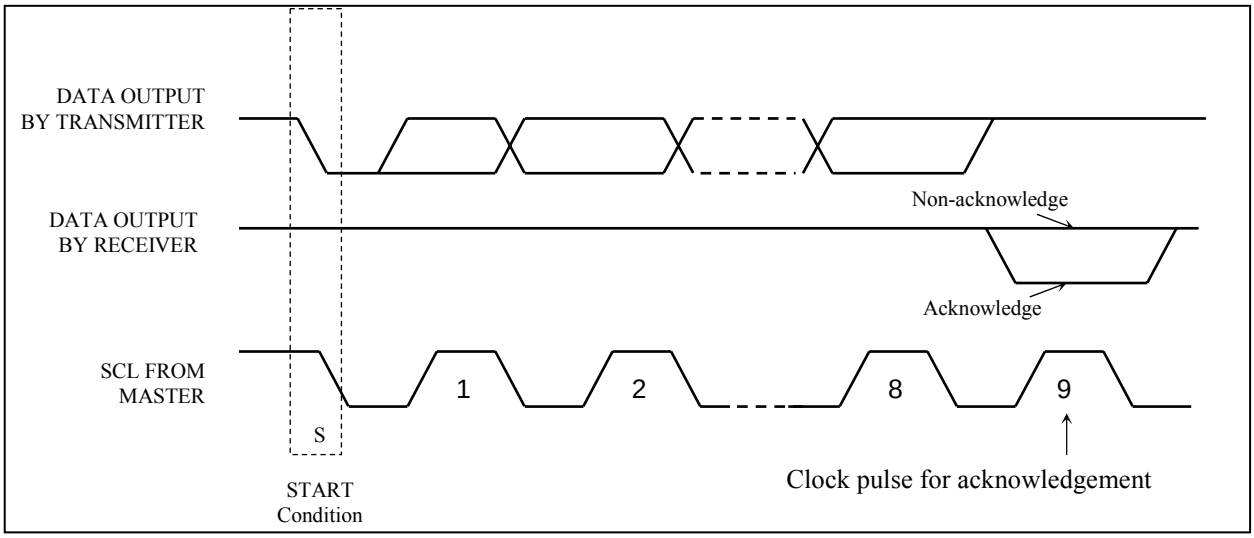


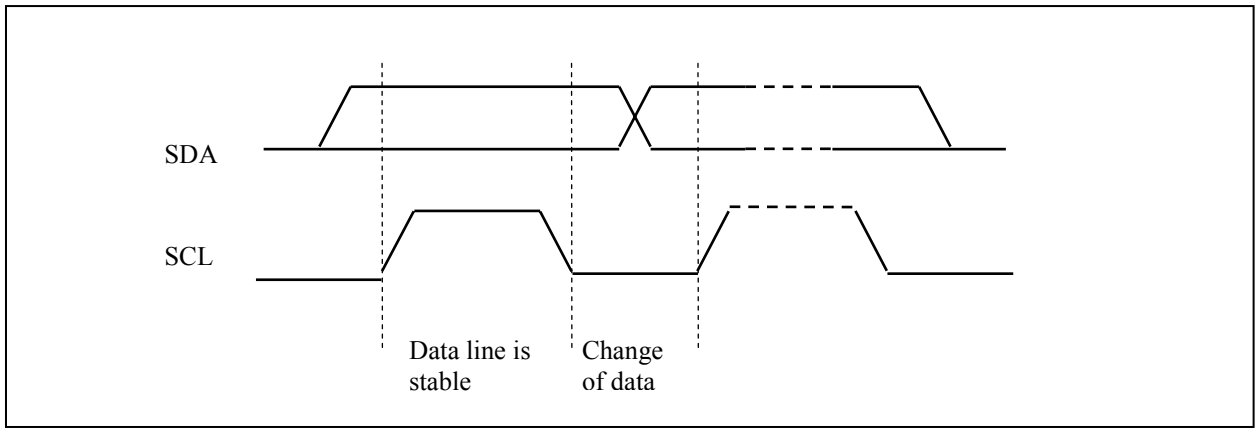
Figure 7-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-10 : Definition of the data transfer condition



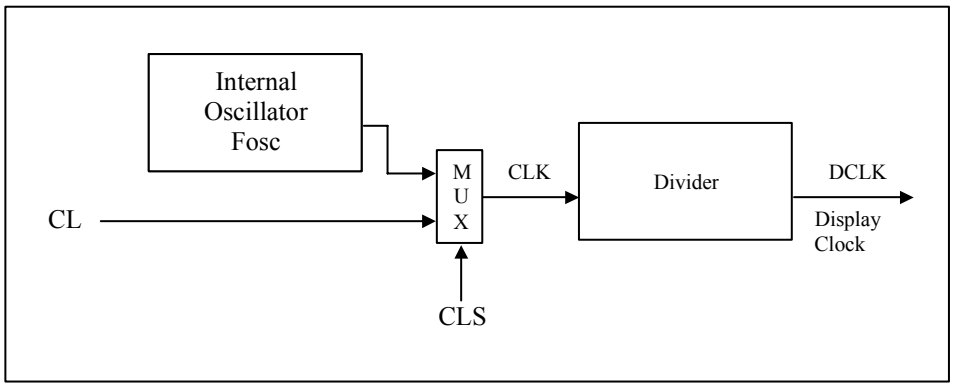
7.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Character Generator RAM (CGRAM) or Display Data RAM (DDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

Figure 7-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

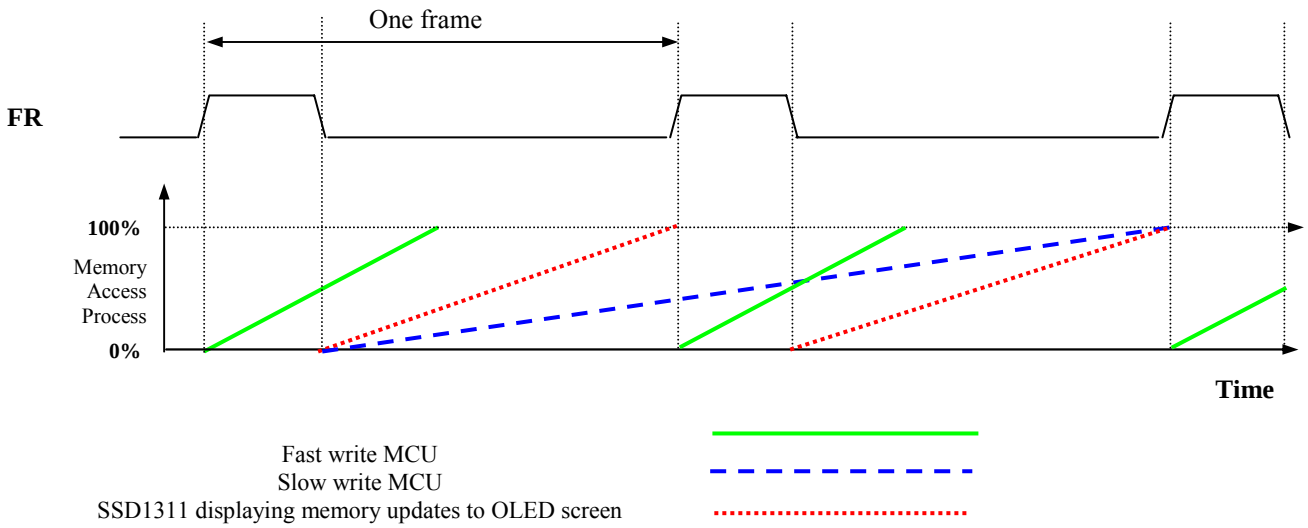
$$F_{FRM} = \frac{F_{osc}}{D \times K \times 1/\text{Duty Ratio}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  = 18 + 7 + 126 = 151 at power on reset (that is K_o is a constant that equals to 126)
  (Please refer to Section 7.5 for the details of the "Phase")
- Duty Ratio depends on display line number; refer to Table 2-1 for details.
- F_{OSC} is the oscillator frequency. It can be changed by OLED command D5h A[7:4]. The higher the register setting results in higher frequency.

7.4 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

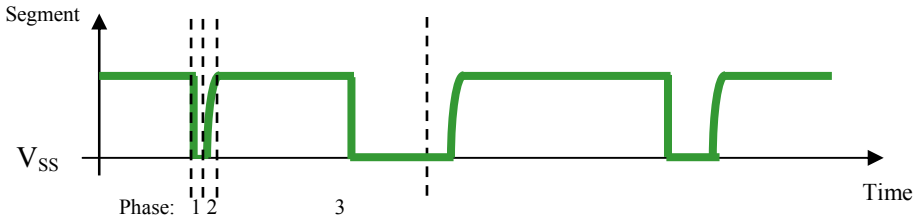
7.5 Segment Drivers / Common Drivers

Segment drivers deliver 100 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 450uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS}. The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 7-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

7.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

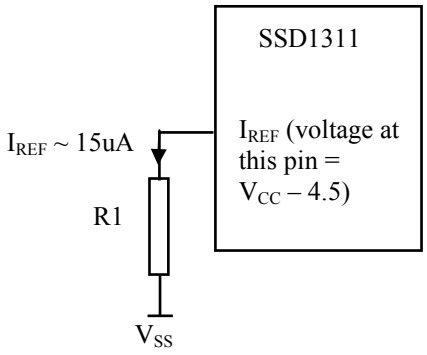
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = (Contrast+1) / 8 x I_{REF}

  in which the contrast (0~255) is set by OLED command "Set Contrast" 81h

  The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 7-13. It is recommended to set I_{REF} to 15 ± 2uA so as to achieve I_{SEG} = 450uA at maximum contrast 255.

Figure 7-13 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} –4.5V, the value of resistor R1 can be found as below:

For I_{REF} = 15uA, V_{CC} =15V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
= (15 – 4.5) / 15uA
= 700kΩ

7.7 Power ON and OFF sequence

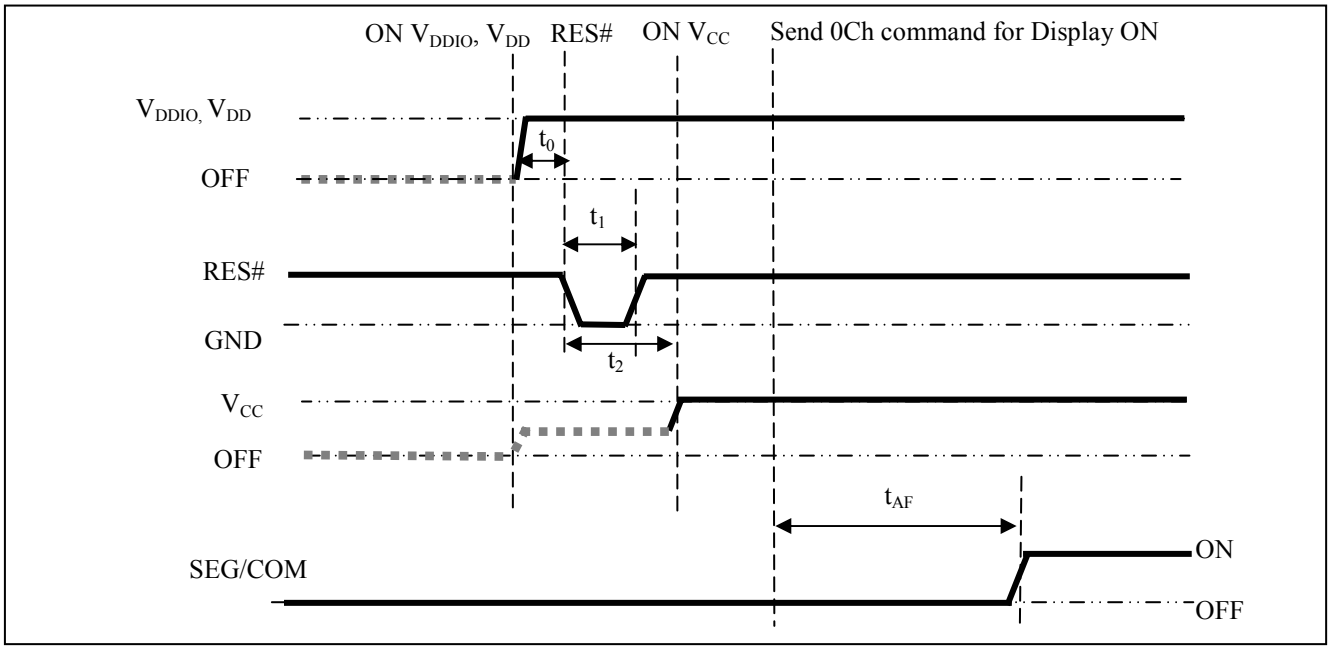
The following figures illustrate the recommended power ON and power OFF sequence of SSD1311 :

When LV I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}, V_{DD}
2. After V_{DDIO}, V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON. SEG/COM will be ON after 100ms (t_{AF}).

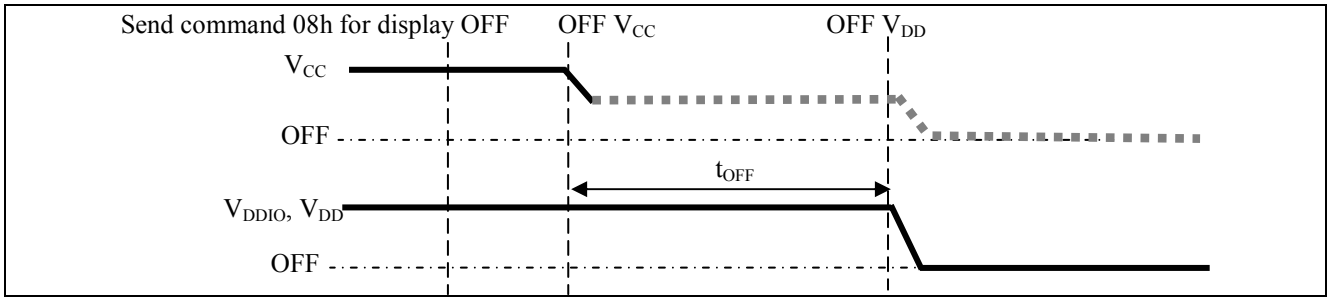
Figure 7-14 : The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DDIO}, V_{DD} after t_{OFF}. (where Minimum t_{OFF}=0ms [5], Typical t_{OFF}=100ms)

Figure 7-15 : The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-14 and Figure 7-15.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

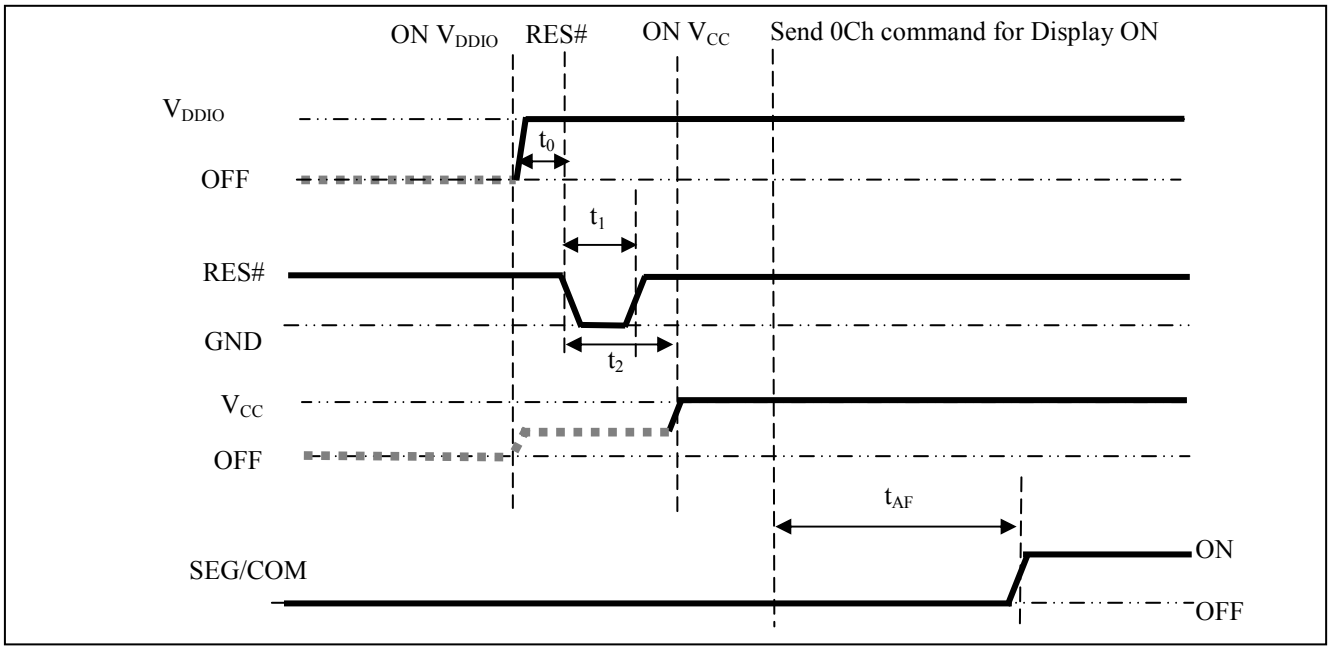
[5] V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

When 5V I/O mode is chosen:

Power ON sequence:

1. Power ON V_{DDIO}
2. After V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send fundamental command 0Ch (for RE=0b, SD=0b) for display ON. SEG/COM will be ON after 200ms (t_{AF}).

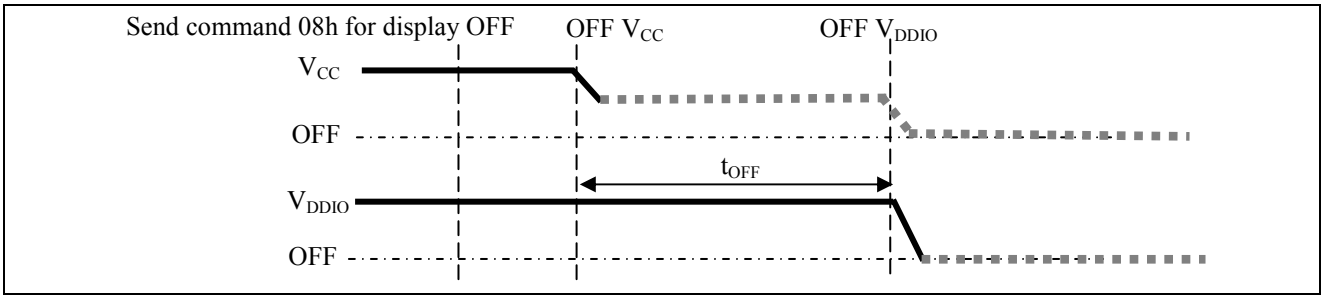
Figure 7-16 : The Power ON sequence



Power OFF sequence:

1. Send fundamental command 08h (for RE=0b, SD=0b) for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DDIO} after t_{OFF}. (where Minimum t_{OFF}=0ms [5], Typical t_{OFF}=100ms)

Figure 7-17 : The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DDIO}, V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DDIO}, V_{DD} whenever V_{DDIO}, V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 7-16 and Figure 7-17.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DDIO}, V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

[5] V_{DDIO}, V_{DD} should not be Power OFF before V_{CC} Power OFF.

7.8 Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when D/C# = Low and R/W# (WR#) = High (Read Instruction Operation), through D7. Before executing the next instruction, be sure that BF is not high.

7.9 Address Counter (AC)

Address Counter (AC) stores DDRAM and CGRAM address, transferred from Command Decoder After writing into (reading from) DDRAM and CGRAM, AC is automatically increased (decreased) by 1. In parallel and serial mode, when D/C# = "Low" and R/W# (WR#) = "High", AC can be read through D[6:0].

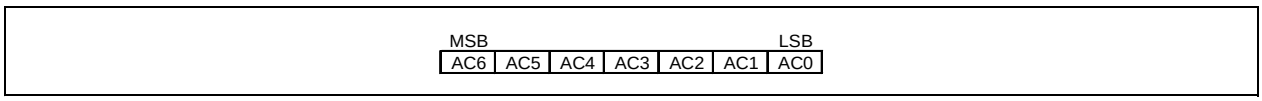
7.10 Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

7.11 Display Data Ram (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 7-18)

Figure 7-18: DDRAM Address

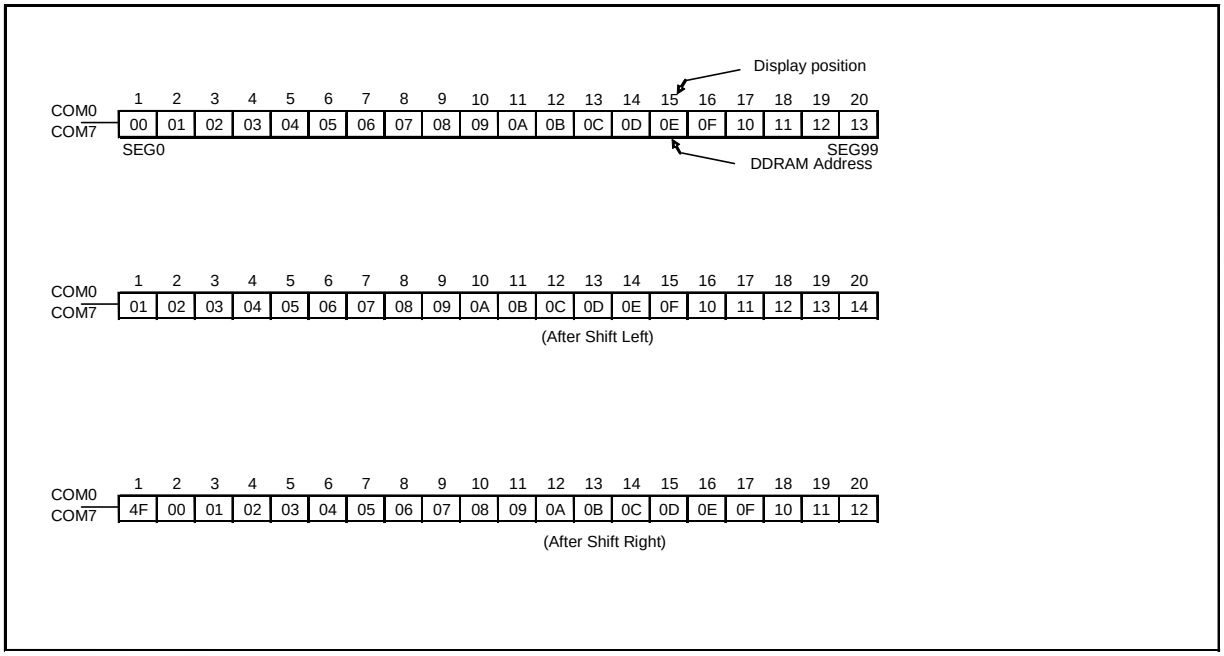


Display of 5-Dot Font Width Character

5-dot 1-line Display

In case of 1-line display with 5-dot font, the address range of DDRAM is 00H-4FH (Refer to Figure 7-19)

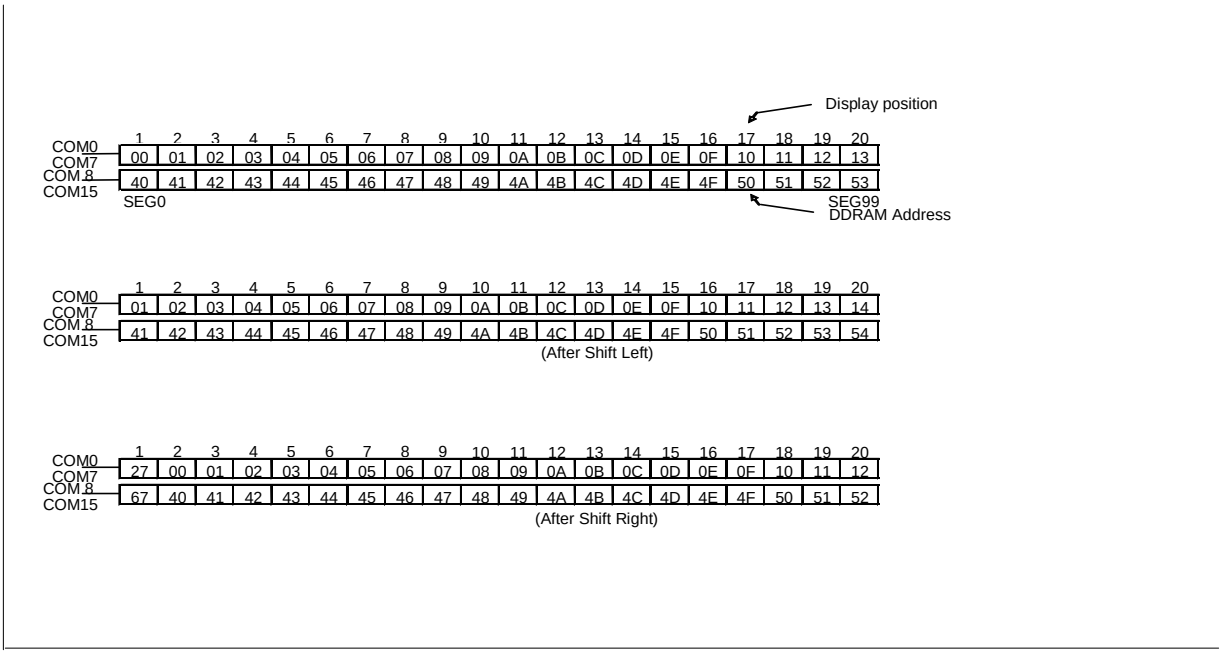
Figure 7-19: 1-line x 20ch. Display (5-dot Font Width)



5-dot 2-line Display

In case of 2-line display with 5-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-20).

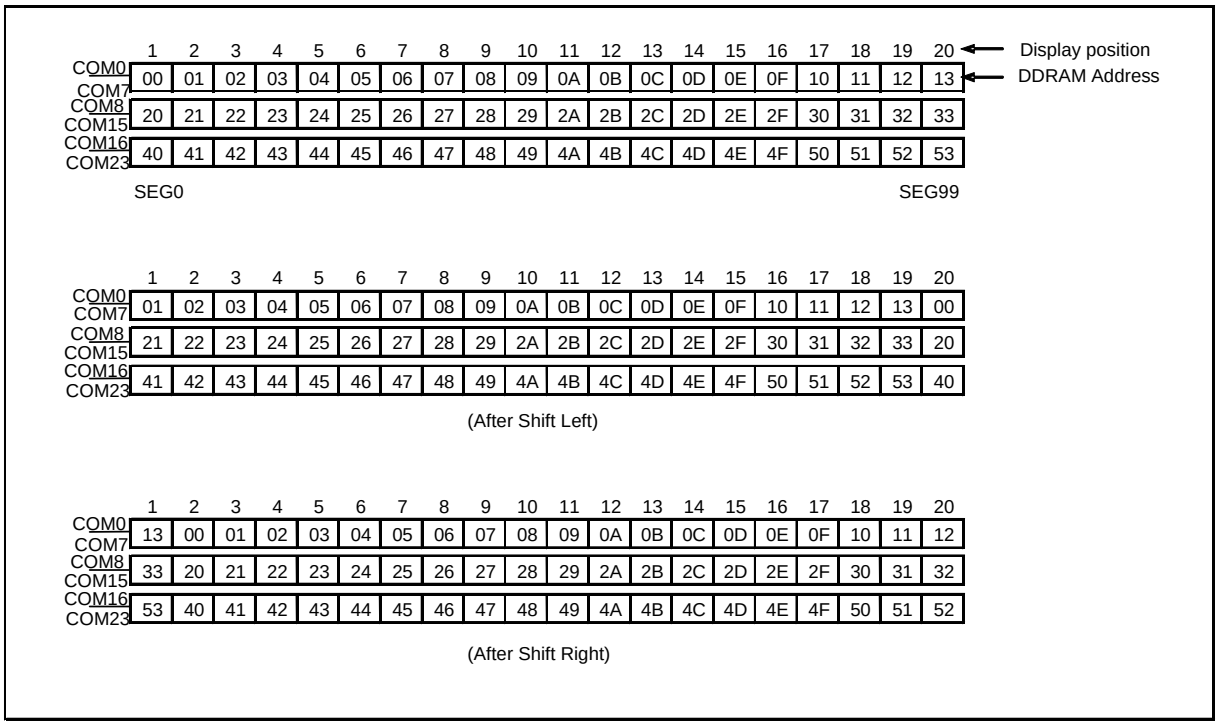
Figure 7-20: 2-line x 20ch. Display (5-dot Font Width)



5-dot 3-line Display

In case of 3-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H (refer to Figure 7-21).

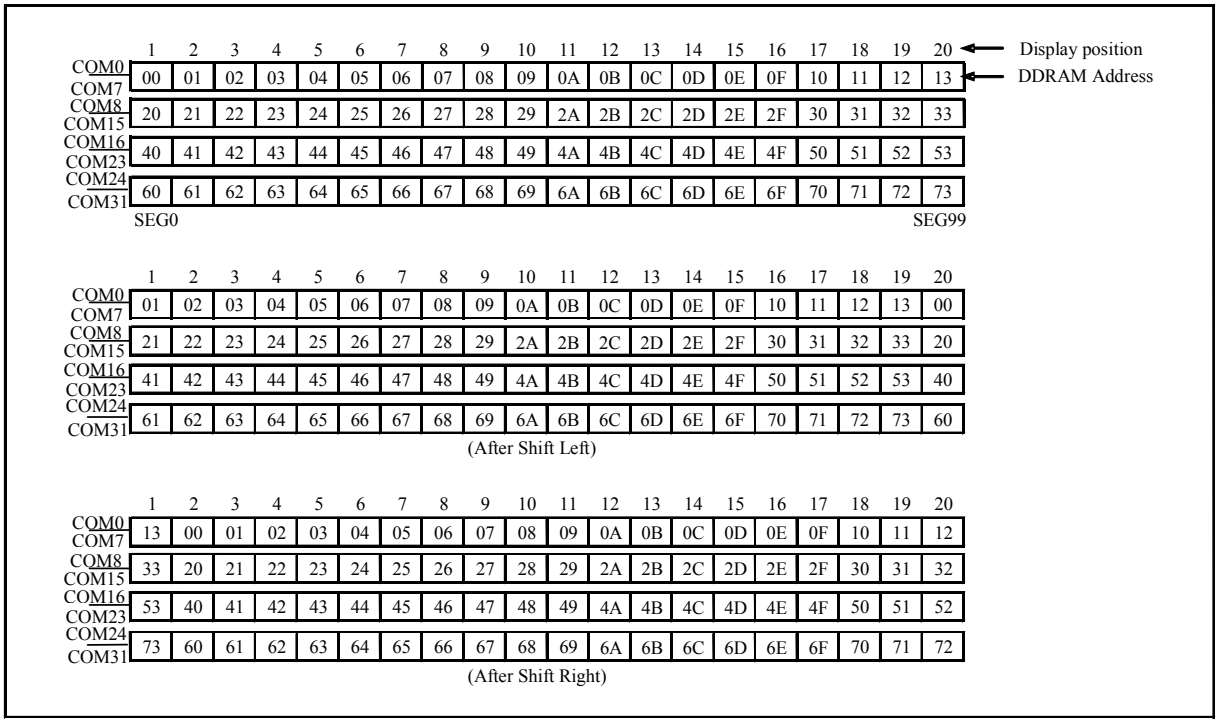
Figure 7-21: 3-line x 20ch. Display (5-dot Font Width)



5-dot 4-line Display

In case of 4-line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-22).

Figure 7-22: 4-line x 20ch. Display (5-dot Font Width)



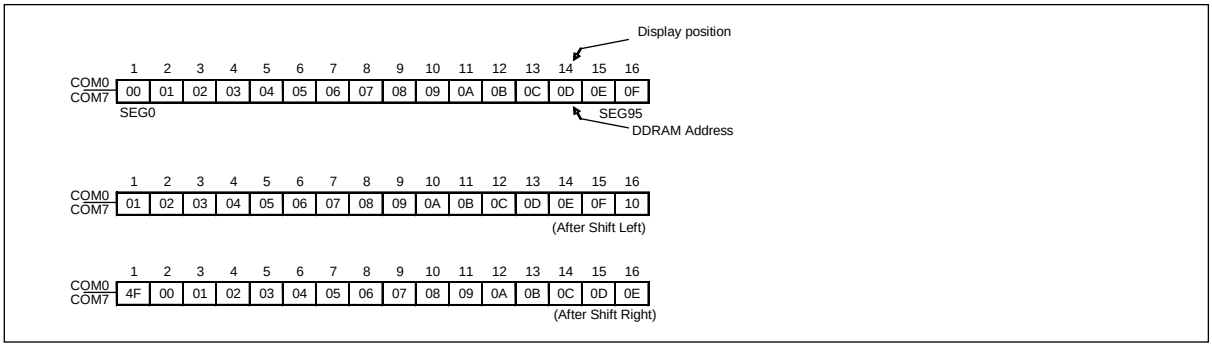
DISPLAY OF 6-DOT FONT WIDTH CHARACTER

When the device is used in 6-dot font width mode, SEG96, SEG97, SEG98 and SEG99 must be opened.

6-dot 1-line Display

In case of 1-line display with 6-dot font, the address range of DDRAM is 00H-4FH (refer to Figure 7-23).

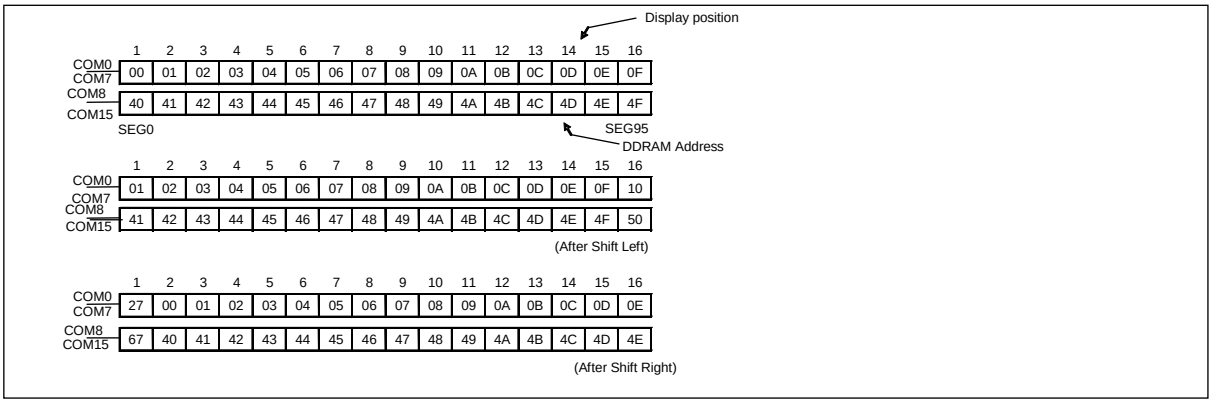
Figure 7-23: 1-line x 16ch. Display (6-dot Font Width)



6-dot 2-line Display

In case of 2-line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 7-24).

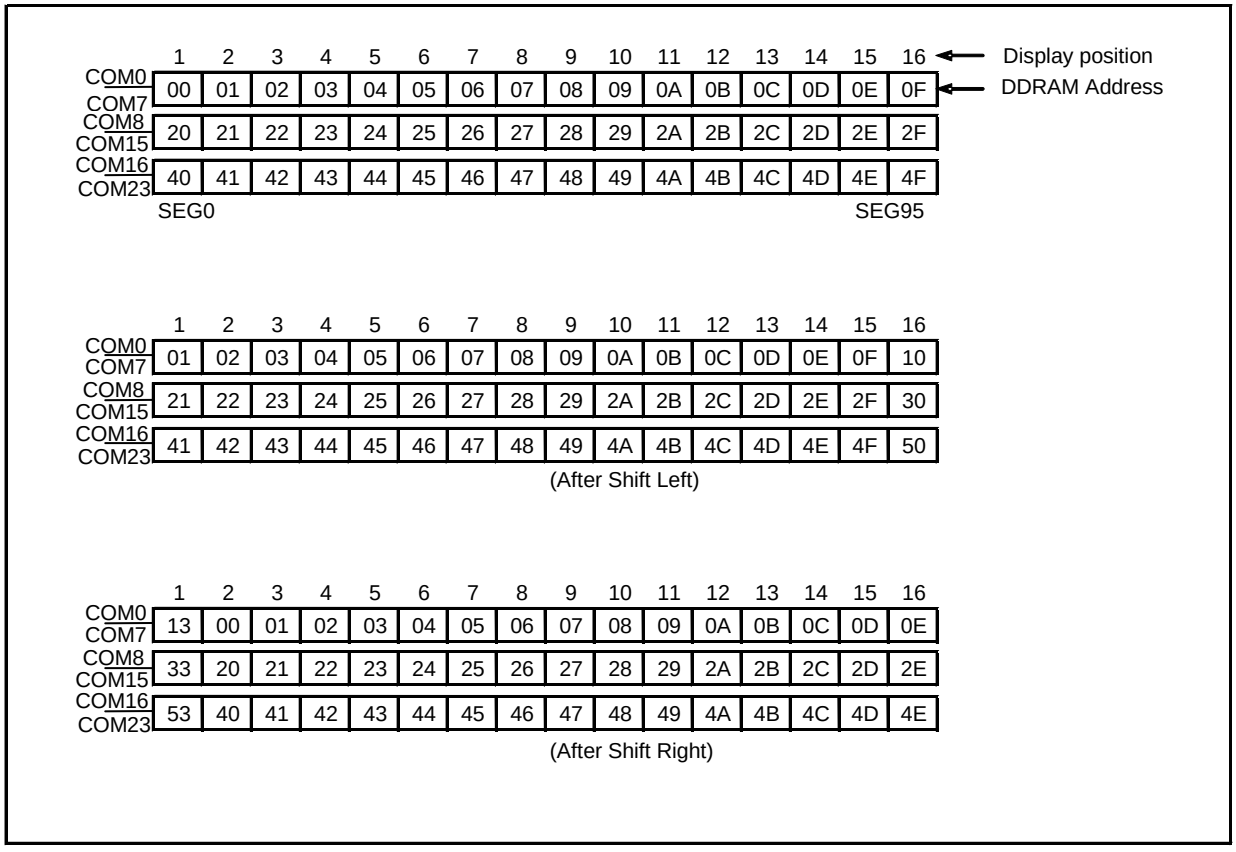
Figure 7-24: 2-line x 16ch. Display (6-dot Font Width)



6-dot 3-line Display

In case of 3-line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H (refer to Figure 7-25).

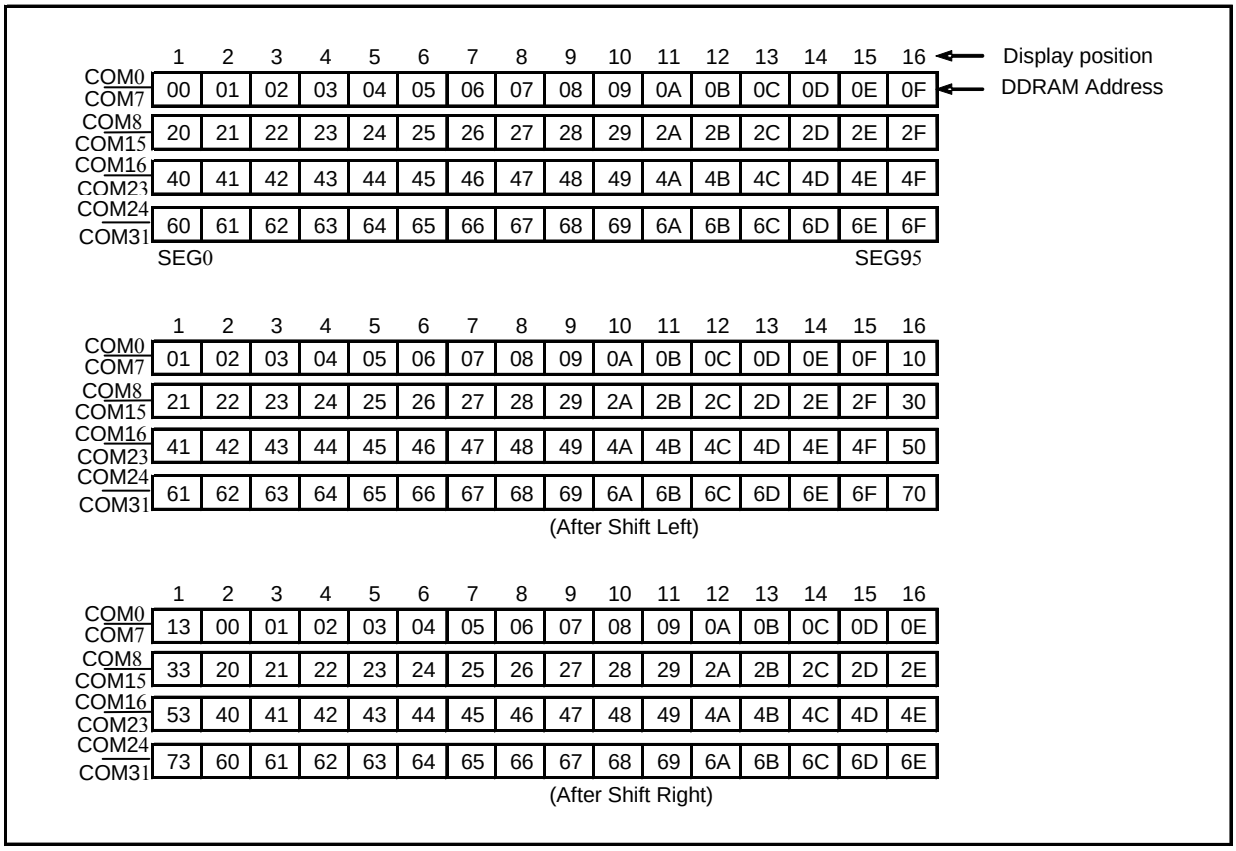
Figure 7-25: 3-line x 16ch. Display (6-dot Font Width)



6-dot 4-line Display

In case of 4-line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 7-26).

Figure 7-26 : 4-line x 16ch. Display (6-dot Font Width)



7.12 CGROM (Character Generator ROM)

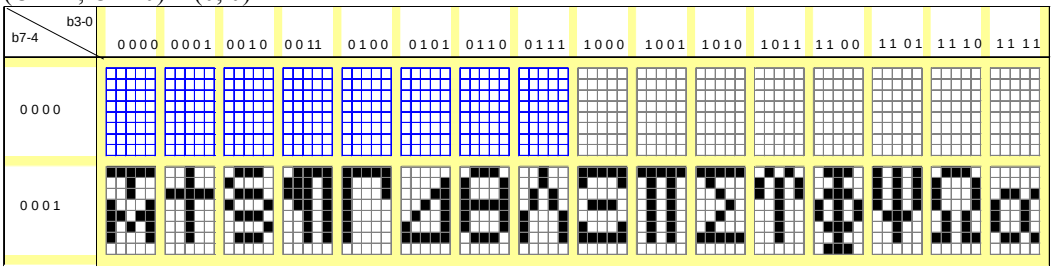
There are 3 optional CGROM's in SSD1311 (details refer to Section 14), which is selected by ROM0 and ROM1 pins (by extension command 72h under appropriate H/W pin setting; refer to Table 6-5 and Table 8-2 for details), while each CGROM has 5 x 8 dots 256 Character Pattern.

7.13 CGRAM (Character Generator RAM)

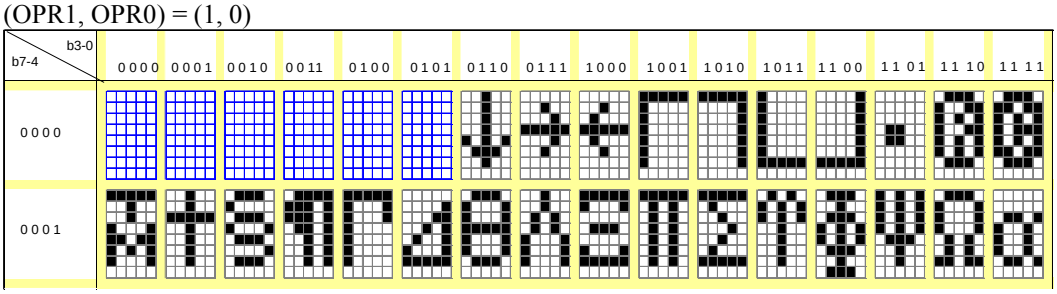
CGRAM has up to 8 characters of 5 x 8 dots, selectable by OPR0 and OPR1 pins (refer to Table 6-6).

Table 7-4: CGRAM and CGROM arrangement with

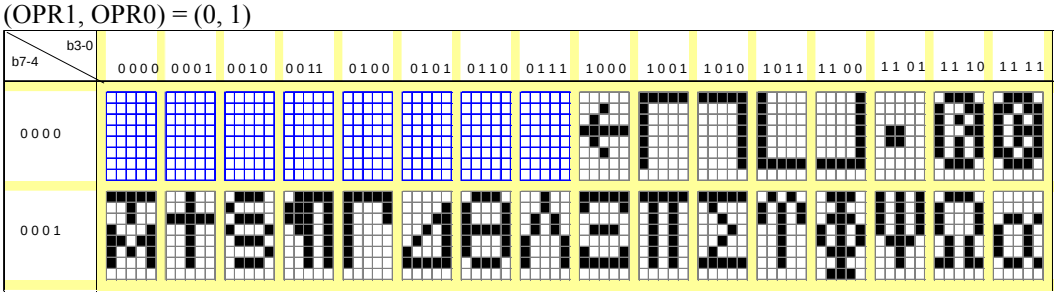
(OPR1, OPR0) = (0, 0)



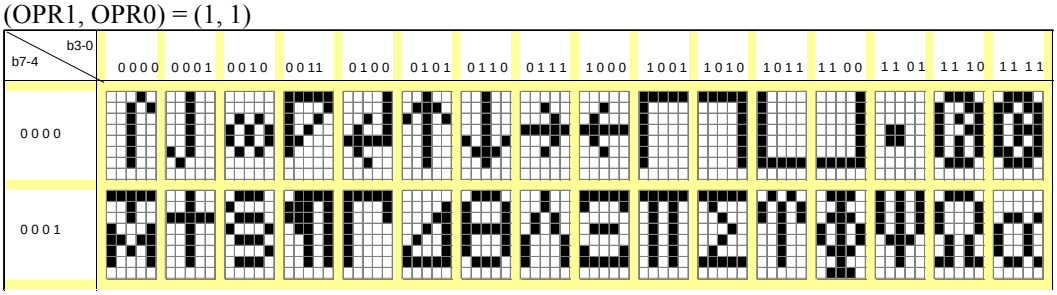
(OPR1, OPR0) = (1, 0)



(OPR1, OPR0) = (0, 1)



(OPR1, OPR0) = (1, 1)



By writing font data to CGRAM, user defined character can be used (refer to Table 7-5).

Table 7-5: Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

5x8 dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	x	0	1	1	1	0	Pattern1
											0	0	1				1	0	0	0	1	
				.							0	1	0				1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0		.		1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.					.			.						.				.
				.					.			.						.				.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	x	1	0	0	0	1	Pattern8
											0	0	1				1	0	0	0	1	
				.					.		0	1	0		.		1	0	0	0	1	
				.					.		0	1	1		.		1	1	1	1	1	
				.					.		1	0	0		.		1	0	0	0	1	
				.					.		1	0	1		.		1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

6 x 8 Dots Character Pattern

Character Code (DDRAM Data)								CGRAM Address						CGRAM Daata								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	Number
0	0	0	0	x	0	0	0	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern1
											0	0	1			0	1	0	0	0	1	
				.							0	1	0			0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0		.	0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	
				.					.			.					.					.
				.					.			.					.					.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	Pattern8
											0	0	1			0	1	0	0	0	1	
				.					.		0	1	0		.	0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	1	1	1	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0			0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	

Notes:

(1) When BE (Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
In case of 5-dot font width, when B1 = "1", enabled dots of P0-P4 will blink, and when B1 = "0" and B0 = "1", enabled dots of P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.
In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.

(2) "X": Don't care

7.14 5V I/O regulator

SSD1311 accepts two low voltage power supply ranges:

- 2.4-3.6V **[Low Voltage I/O Application]** and
- 4.4-5.5V **[5V I/O Application]**

5V IO Regulator is enabled to regulate internal V_{DD} for power supply of internal circuit blocks (core logic operation).

Table 7-6 summarizes the input / output connection of 5V IO regulator in normal application.

Table 7-6: 5V IO regulator pin description

Pin Name	Low Voltage I/O Application	5V I/O Application
REGVDD	LOW, disable 5V I/O regulator	HIGH, enable 5V I/O regulator
V_{DD}	2.4 - V_{DDIO}	NC with stabilizing capacitor It is intenally regulated
V_{DDIO}	2.4V -3.6V	4.4V -5.5V

8 COMMAND TABLE

There are three sets of command set in SSD1311: Fundamental Command Set, Extended Command Set and OLED Command Set. These three command sets can be selected by setting logic bits IS, RE and SD accordingly.

Table 8-1: Fundamental Command Table

1. Fundamental Command Set														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Clear Display	**X**	**X**	**0**	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	**X**	**0**	**0**	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	**X**	**0**	**0**	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	**1**	**0**	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON / OFFControl	**X**	**0**	**0**	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). **Note:** It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance; refer to Section 9.1.4 for details

1. Fundamental Command Set														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Extended Function Set	**X**	**1**	**0**	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR) NW = "1": 3-line or 4-line display mode (POR) NW = "0": 1-line or 2-line display mode
Cursor or Display Shift	**0**	**0**	**0**	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left
Double Height (4-line) / Display-dot shift	**0**	**1**	**0**	0	0	0	0	0	1	UD2	UD1	*	DH'	UD2~1: Assign different doubt height format (POR=11b) Refer to Table 9-2 for details DH' = "1": display shift enable DH' = "0": dot scroll enable (POR)
Shift Enable	**1**	**1**	**0**	0	0	0	0	0	1	DS4	DS3	DS2	DS1	DS[4:1]=1111b (POR) when DH' = 1b Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.
Scroll Enable	**1**	**1**	**0**	0	0	0	0	0	1	HS4	HS3	HS2	HS1	HS[4:1]=1111b (POR) when DH' = 0b Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.

1. Fundamental Command Set														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Function Set	**X**	**0**	**0**	0	0	0	0	1	*	N	DH	**RE (0)**	**IS**	Numbers of display line, N when N = "1" (POR): 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = " 1/0": Double height font control for 2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS
	X	**1**	**0**	0	0	0	0	1	*	N	BE	**RE (1)**	REV	CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)
Set CGRAM address	**0**	**0**	**0**	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	**X**	**0**	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	**X**	**1**	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	**X**	**X**	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	**X**	**X**	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	**X**	**X**	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

Notes

(1) POR stands for Power On Reset Values.

(2) "*" and "X" stand for "Don't care".

Table 8-2: Extended Command Table

2. Extended Command Set															
Command	**IS**	**RE**	**SD**	**Instruction Code**											**Description**
				D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Function Selection A	**X**	**1**	0	0	0	71	0	1	1	1	0	0	0	1	A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)
	X	**1**	0	1	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Function Selection B	**X**	**1**	0	0	0	72	0	1	1	1	0	0	1	0	OP[1:0]: Select the character no. of character generator RO[1:0]: Select character ROM **Note:** It is recommended to turn off the disply (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards
	X	**1**	0	1	0		*	*	*	*	RO1	RO0	OP1	OP0	
OLED Characterization	**X**	**1**	X	0	0	78 / 79	0	1	1	1	1	0	0	SD	Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 8-3.

OP[1:0]	CGROM	CGRAM
00b	240	8
01b	248	8
10b	250	6
11b	256	0

RO[1:0]	ROM
00b	A
01b	B
10b	C
11b	Invalid

Notes
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

Table 8-3: OLED Command Table

3. OLED Command Set														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Set Contrast Control	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)
Set Display Clock Divide Ratio/Oscillator Frequency	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1 (POR=0000b) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value ncreases.
Set Phase Length	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	A[3:0] : Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4] : Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b)
Set SEG Pins Hardware Configuration	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 0	0 0	A[4]=0b, Sequential SEG pin configuration A[4]=1b (POR), Alternative (odd/even) SEG pin configuration A[5]=0b (POR), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap Refer to Table 8-4 for details
Set V_{COMH} Deselect Level	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	A[6:4] / Hex code / V_{COMH} deselect level 000b / 00h / ~ 0.65 x V_{CC} 001b / 10h / ~ 0.71 x V_{CC} 010b / 20h / ~ 0.77 x V_{CC} (POR) 011b / 30h / ~ 0.83 x V_{CC} 100b / 40h / 1 x V_{CC}

3. OLED Command Set

<table>
<tr><th rowspan="2">Command</th><th>IS</th><th>RE</th><th>SD</th><th colspan="10">Instruction Code</th><th rowspan="2">Description</th></tr>
<tr><th></th><th></th><th></th><th>D/C#</th><th>R/W# (WR#)</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Function Selection C</td><td>X
X</td><td>1
1</td><td>1
1</td><td>0
0</td><td>0
0</td><td>DC
A[7:0]</td><td>1
A_7</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
0</td><td>1
0</td><td>0
A_1</td><td>0
A_0</td><td>Set VSL & GPIO

Set VSL:
A[7] = 0b: Internal VSL (POR)
A[7] = 1b: Enable external VSL

Set GPIO:
A[1:0] = 00b represents GPIO pin HiZ, input disabled (always read as low)
A[1:0] = 01b represents GPIO pin HiZ, input enabled
A[1:0] = 10b represents GPIO pin output Low (RESET)
A[1:0] = 11b represents GPIO pin output High</td></tr>
<tr><td>Set Fade Out and Fade in / out</td><td>X
X</td><td>1
1</td><td>1
1</td><td>0
0</td><td>0
0</td><td>23
A[5:0]</td><td>0
*</td><td>0
*</td><td>1
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET]

A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled.

A[5:4] = 11b Enable Fade in / out mode.
Once Fade in / out mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Fade in / out mode is disabled.

A[3:0] : Set time interval for each fade step

<table><tr><th>A[3:0]</th><th>Time interval for each fade step</th></tr><tr><td>0000b</td><td>8 Frames</td></tr><tr><td>0001b</td><td>16 Frames</td></tr><tr><td>0010b</td><td>24 Frames</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1110b</td><td>120 Frames</td></tr><tr><td>1111b</td><td>128 Frames</td></tr></table></td></tr>
</table>

Note

(1) POR stands for Power On Reset Values.

(2) "*" and "X" stand for "Don't care".

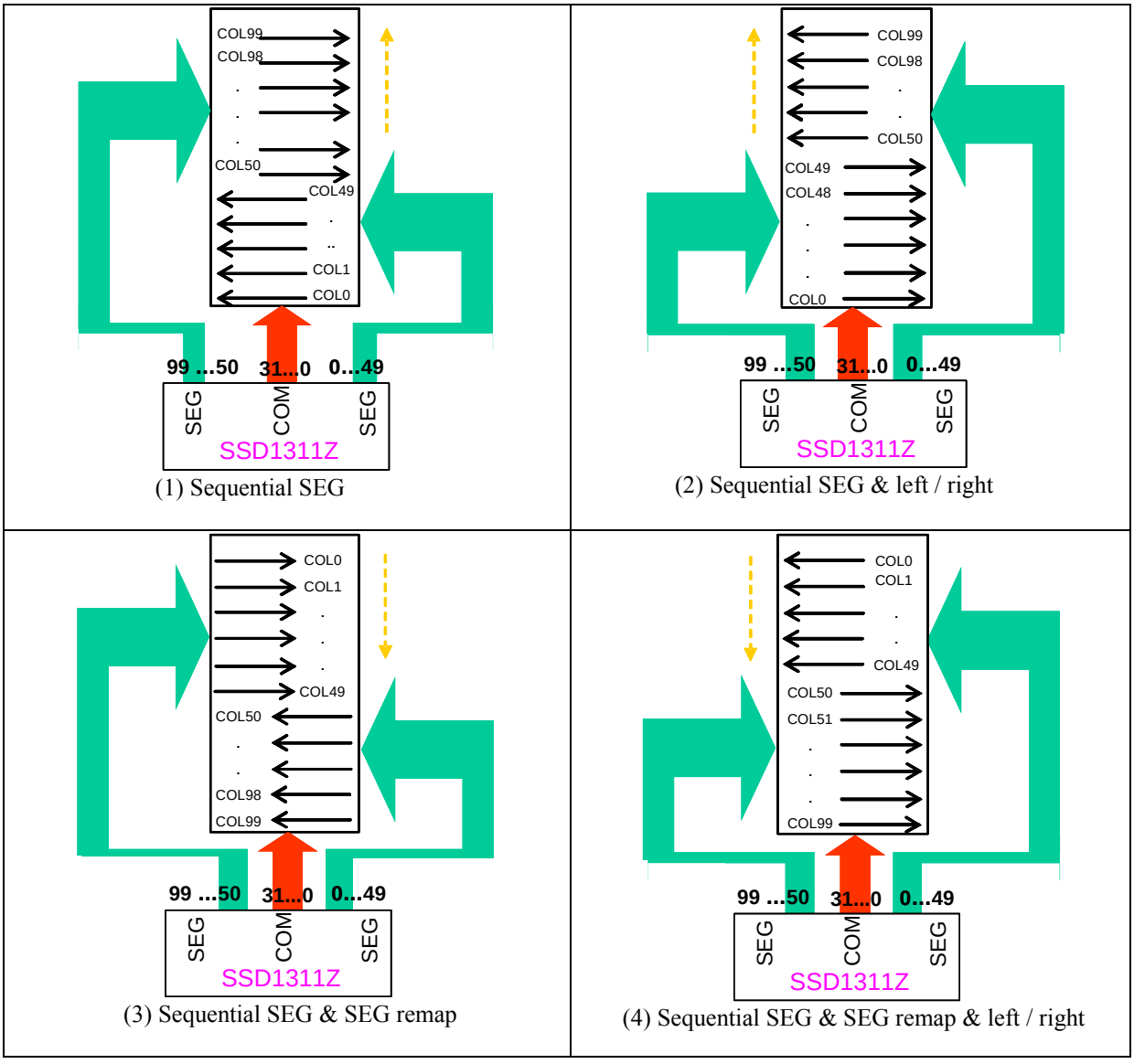
(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.

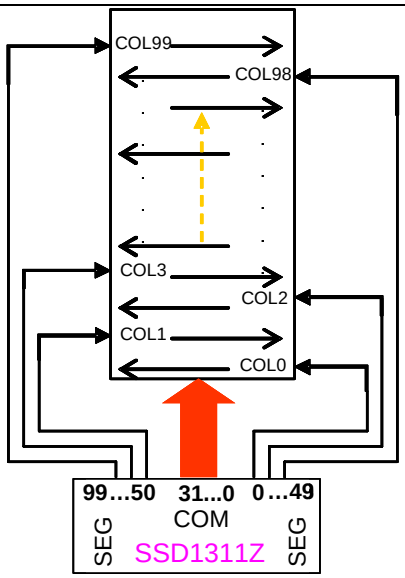
(4) Refer to Table 8-1 and Table 8-2 for the details of logic bits IS, RE and SD.

Table 8-4 : SEG Pins Hardware Configuration

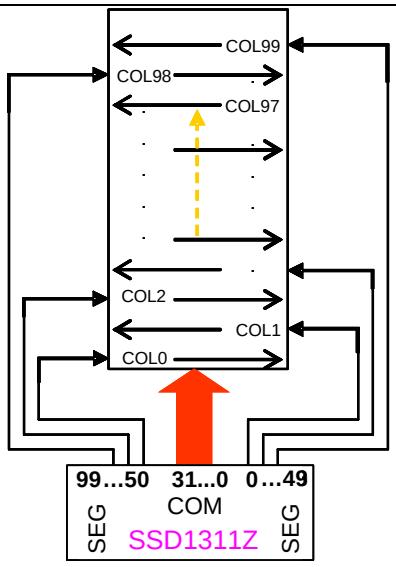
SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

Case no.	Oddeven (1) / Sequential (0) OLED Command : DAh -> A[4]	SEG Remap (Fundamental) Command Control bit: BDS; or by H/W setting: SHLS	Left / Right Swap OLED Command : DAh -> A[5]	Remark
1	0	1	0	
2	0	1	1	
3	0	0	0	
4	0	0	1	
5	1	1	0	Default
6	1	1	1	
7	1	0	0	
8	1	0	1	

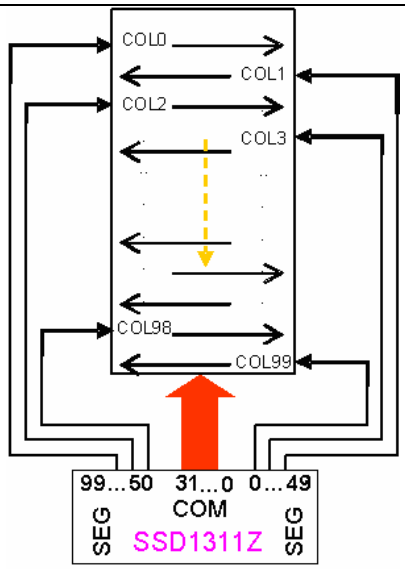




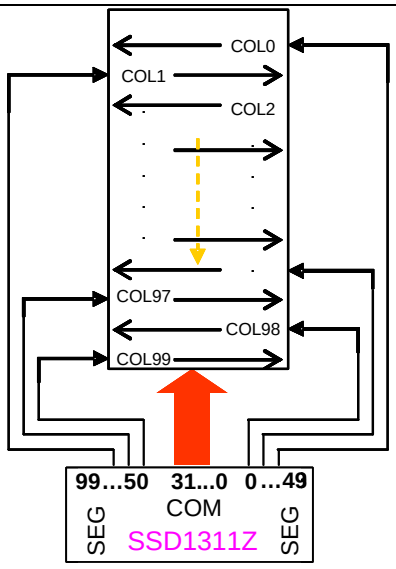
(5) Odd / even SEG



(6) Odd / even SEG & left / right



(7) Odd / even SEG & SEG remap



(8) Odd / even SEG & SEG remap & left / right

Note:
(1) The above eight figures are all with bump pads being faced up.

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command Set

9.1.1 Clear Display (IS= X, RE = X, SD = 0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

9.1.2 Return Home (IS= X, RE = 0, SD = 0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

9.1.3 Entry Mode Set (IS= X, RE = 0 or 1, SD = 0)

When RE = 0

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

- CGRAM operates the same as DDRAM, when read from or write to CGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the command “Shift Enable” is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM read/write operation, shift of display like this function is not performed.

When RE = 1

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	BDC	BDS

Set the data shift direction of segment in the application set.

BDS: Data shift direction of segment
When BDS = "Low", segment data shift direction is set to reverse from SEG99 to SEG0.
When BDS = "High", segment data shift direction is set to normal order from SEG0 to SEG99.

BDC: Data shift direction of common
When BDC = "Low", common data shift direction is set to reverse from COM31 to COM0.
When BDC = "High", common data shift direction is set to normal order from COM0 to COM31.

The BDC, BDS setting is recommended to be set at the same time as the command “Function set”.

9.1.4 Display ON/OFF Control (IS= X, RE = 0, SD = 0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned ON.
When D = "Low", display is turned OFF, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit
When C = "High", cursor is turned ON.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is ON, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is OFF.

It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance, see the below S/W code setting for reference (assume 2-line application and the display contents have to be updated repeatedly):

```
For loop {
        cmd 28h
        cmd 0Ch          // disable cursor & blinking during display on
        cmd 80h          // define DDRAM address to update RAM for display line #1
        write data x 20 char
        cmd C0h          // define DDRAM address to update RAM for display line #2
        write data x 20 char
        cmd 80h                  // define DDRAM address to let the cursor & blinking effect appears on the 1st char
                                 of the 1st display line after refreshing / updating the whole display
        cmd 0Fh          // enable cursor & blinking during display on
        }
```

9.1.5 Extended Function Set (IS= X, RE = 1, SD = 0)

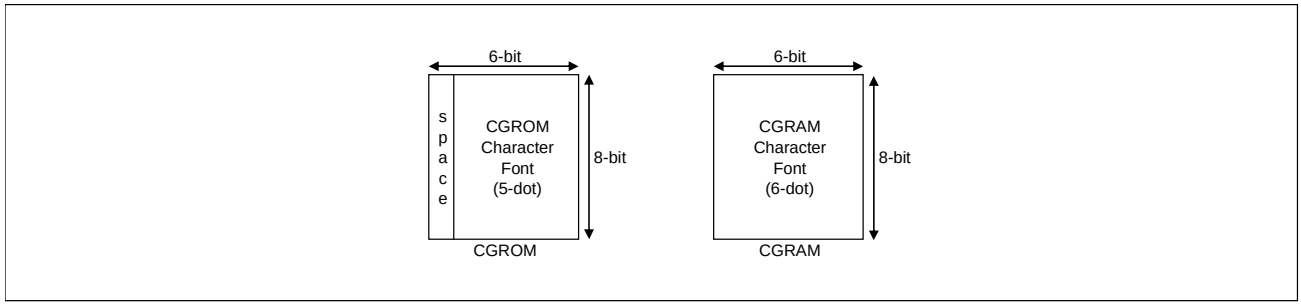
D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FW	B/W	NW

FW: Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(refer to Figure 9-1)
When FW = "Low", 5-dot font width is set.

B/W: Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit in the command “Display ON/OFF Control” becomes don't care condition.

NW: 4 Line mode enable bit
When NW = "High", 3 or 4 line display mode is set. In this case, N bit in the command “Function set” becomes don't care condition.
When NW = "Low", 1 or 2 line display mode is set. In this case, N bit in the command “Function set” becomes don't care condition.

Figure 9-1 : 6-dot Font Width CGROM/CGRAM



9.1.6 Cursor or Display Shift (IS = 0, RE = 0, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	S/C	R/L	X	X

Shift right / left cursor position or display, without writing or reading of display data. This command is used to correct or search display data (refer to Table 9-1). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. When 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line enabled by DS1-DS4 in the command "Shift Enable". When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

Table 9-1: Shift patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1.
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display. No change in address counter.
1	1	Shift all the display to the right, cursor moves according to the display. No change in address counter.

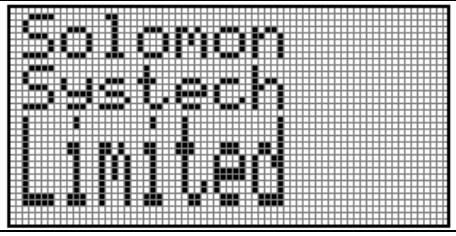
9.1.7 Double Height (4-line) / Display-dot shift (IS = 0, RE = 1, SD = 0)

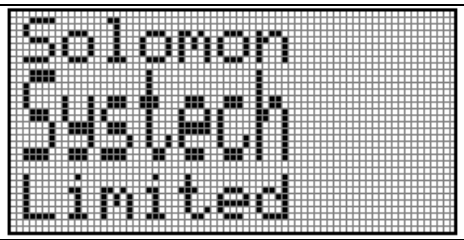
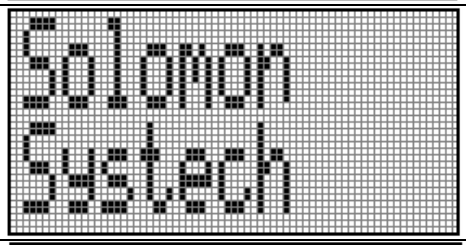
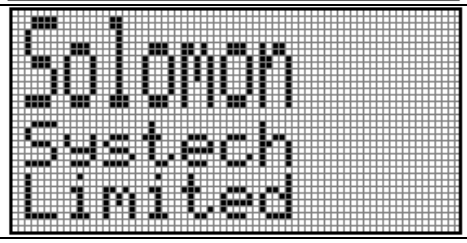
D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	UD2	UD1	X	DH'

UD2, UD1: Assign different double height formats, they are applicable to different line display modes when DH bit in command "Function Set" =1.

Note that UD1=0 and UD2=0 are forbidden in 2-line display mode, while UD1=0 is forbidden in 3-line display mode.

Table 9-2: Double Height Display According to UD2 andUD1 Bits (when DH=1)

UD2	UD1	Character Displays
0	0	

0	1	
1	0	
1	1	

DH': Display shift enable selection bit.
When DH' = "High", display shift per line enabled.
When DH' = "Low", smooth dot scroll enabled.

9.1.8 Shift/Scroll Enable (IS =1, RE = 1, SD=0)

Shift Enable - DH' = 1

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display shift per line enable this instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.
If DS1 and DS2 are set to "High" (enable) in 2 line mode, 1st line and 2nd line are shifted. If all the DS bits (DS1 to DS4) are set to "Low" (disable), no shift is observed on the display.

Scroll Enable - DH' = 0

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal scroll per line enable
This command makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If scroll the line in 1-line display mode, set HS1 to "High".
If the 2nd line scroll is needed in 2-line mode, set HS2 to "High" (refer to Table 9-3).

Note: DH' bit is in command "Double Height (4-line) / Display-dot shift"

Table 9-3: Relationship between DS and COM signal

Enable Bit	Enabled Common Signals During Shift	Description
HS1 / DS1	COM1 – COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2 / DS2	COM9 – COM16	
HS3 / DS3	COM17 – COM24	
HS4 / DS4	COM25 – COM32	

9.1.9 Function Set (IS = X, RE = 0 or 1, SD = 0)

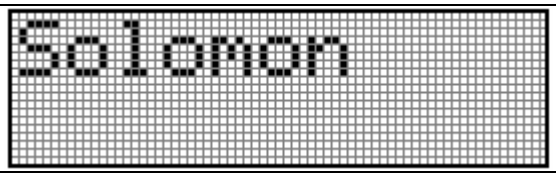
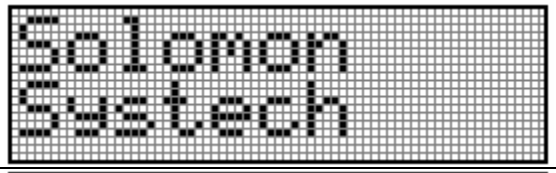
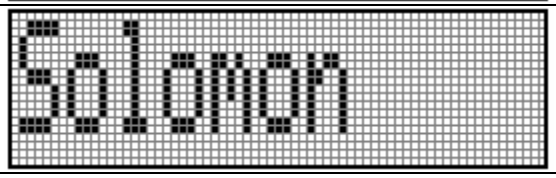
RE = 0

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	X	N	DH	RE(0)	IS

N: Display line number control bit
When N = "Low", 1-line display mode (for NW=0), or 3-line display mode (for NW=1).
When N = "High", 2-line display mode is set (for NW=0), or 4-line display mode (for NW=1).

DH: When DH= "High", UD2=1 and UD1=1 Double height font type control bit for 2 line mode:

Table 9-4: Double Height display when DH=1, UD2=1 and UD1=1

NW	N	DH	Display lines	Character font	Character Displays
0	0	0	1	5 x 8	
0	0	1	1	Forbidden	
0	1	0	2	5 x 8	
0	1	1	2	5 x 16	

When DH= "Low", Double height font type control is disabled.

RE: Extended function registers enable bit
At this instruction, RE must be "Low".

IS: Special registers enable bit

RE = 1

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	X	N	BE	RE(1)	REV

N: Display line number control bit
When N = "Low", 1-line display mode (for NW=0), or 3-line display mode (for NW=1).
When N = "High", 2-line display mode is set (for NW=0), or 4-line display mode (for NW=1).

BE: CGRAM data blink enable bit
If BE is "High", it makes user font of CGRAM blink. The quantity of blink is assigned at the highest 2 bit of CGRAM. If BE is "Low" CGRAM blink is disabled.

RE: Extended function registers enable bit
At this instruction, RE must be "High".
When RE = "High", the following control bits / commands can be accessed:
- BDC/ BDS control bits of Entry Mode Set command,
- HS / DS control bits of Shift / Scroll enable commands,
- UD2/UD1/DH' control bits of Double height (4-line) / Display-dot Shift command,
- SQ control bits of Set Scroll Quantity command, and
- BE / REV control bits of function set register can be accessed.

REV: Reverse enable bit

When REV = “High”, all the display data are reversed. Namely, all the white dots become black and black dots become white.

When REV = “Low”, the display mode set normal display.

9.1.10 Set CGRAM Address (IS = 0, RE = 0, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This command makes CGRAM data available from MPU.

9.1.11 Set DDRAM Address (IS = X, RE = 0, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This command makes DDRAM data available from MPU.

- In 1-line display mode (N = 0, NW = 0), DDRAM address is from “00H” to “4FH”.
- In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from “00H” – “27H”, and DDRAM address in the 2nd line is from “40H” – “67H”.
- In 3-line display mode (N=0, NW = 1), DDRAM address is from “00H” – “13H” in the 1st line, from “20H” to “33H” in the 2nd line and from “40H” – “53H” in the 3rd line.
- In 4-line display mode (N=1, NW = 1), DDRAM address is from “00H” – “13H” in the 1st line, from “20H” to “33H” in the 2nd line, from “40H” – “53H” in the 3rd line and from “60H” – “73H” in the 4th line.

Details refer to Section 7.11.

9.1.12 Set Scroll Quantity (IS = X, RE = 1, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units (Refer to Table 9-5). In this case SSD1311 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Table 9-5: Scroll Quantity According to HDS Bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
0	0	0	0	1	1	Shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	Shift left by 47-dot
1	1	X	X	X	X	Shift left by 48-dot

9.1.13 Read Busy Flag & Address (IS = X, RE = X, SD=0)

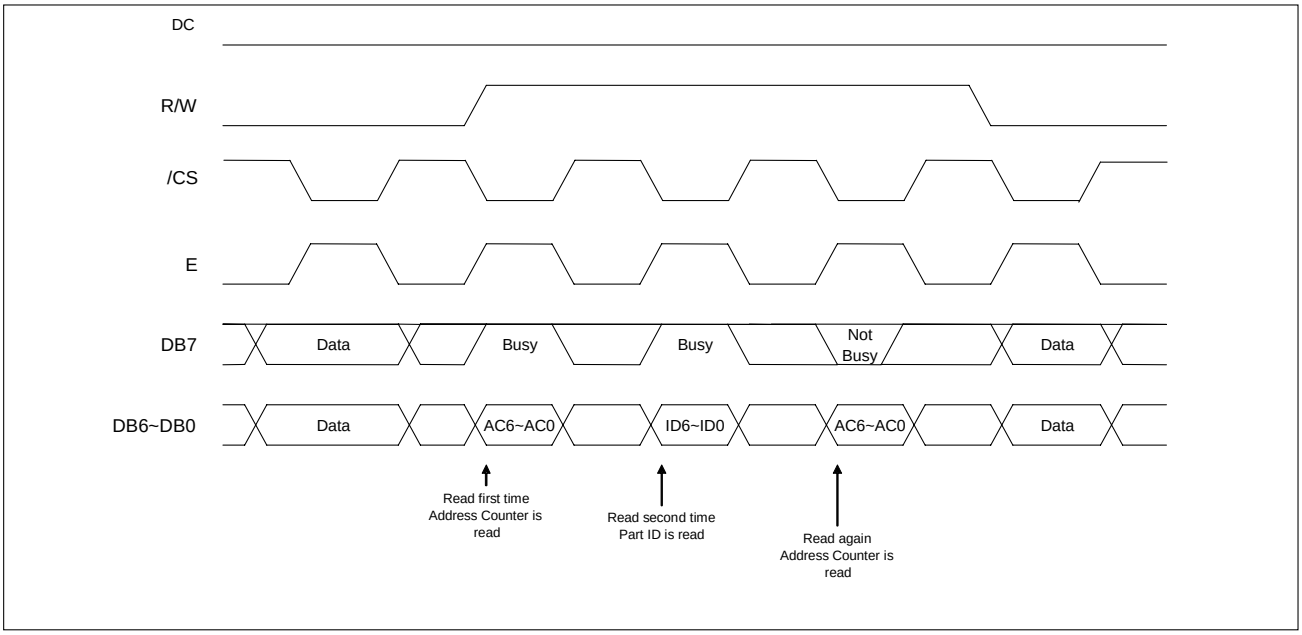
D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BF	AC6/ID6	AC5/ID5	AC4/ID4	AC3/ID3	AC2/ID2	AC1/ID1	AC0/ID0

This command shows whether SSD1311 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress . Then wait until BF is Low before the next instruction can be performed.

The value of address counter or the part ID can be read through this command. When first time run this command, the address counter can be read. When this command is run for second time, the part ID can be read (refer to Figure 9-2).

Part Number	Part ID
SSD1311	0100001

Figure 9-2: Read Busy Flag & Address/Part ID (6800 – parallel interface)



9.1.14 Write Data to RAM (IS = X, RE = X, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM or CGRAM is set by the previous address setting command: “Set DDRAM address” or “Set CGRAM address”. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased / decreased by 1, according to the entry mode.

9.1.15 Read Data from RAM (IS = X, RE = X, SD=0)

D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined.

If RAM data is read several times without RAM address set instruction before read operation, correct RAM data can be got from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but only the previous data can be read by read instruction.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read.

9.2 Extended Command Set

9.2.1 Function Selection A [71h] (IS = X, RE = 1, SD=0)

This double byte command enable or disable the internal V_{DD} regulator at 5V I/O application mode.
The internal V_{DD} is enabled as default by data 5Ch, whereas it is disabled if the data sequence is set as 00h.

9.2.2 Function Selection B [72h] (IS = X, RE = 1, SD=0)

Beside using ROM[1:0] and OPR[1:0] hardware pins, the character number of the Character Generator RAM and the character ROM can be selected through this command, details refer to Table 8-2.

It is recommended to turn off the disply (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards

9.2.3 OLED Characterization [78H/ 79h] (IS = X, RE = 1, SD= 0 or 1)

This single byte command is used to select the OLED command set. When SD is set to 0b , OLED command set is disabled. When SD is set to 1b, OLED command set is enabled.

9.3 OLED Command Set

9.3.1 Set Contrast Control (81h)

This command sets the Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases as the contrast step value increases.

9.3.2 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D)(A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 7.3 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings. The default setting is 0111b.

9.3.3 Set Phase Length (D9h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 2 to 32 in the unit of DCLKs.

- Phase 2 (A[7:4]): Set the period from 1 to 15 in the unit of DCLKs.

9.3.4 Set SEG Pins Hardware Configuration (DAh)

This double byte command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 8-4.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

9.3.5 Set V_{COMH} Deselect Level (DBh)

This command adjusts the V_{COMH} regulator output.

9.3.6 Set VSL / GPIO (DCh)

This double byte command consists of two functions:

- Set VSL (A[7])
  External VSL is enabled when A[7] is set to 1b, whereas it is set to internal VSL as default at A[7] = 0b.

- Set the states of GPIO (A[1:0])
  The state of GPIO can be defined by control bits A[1:0]; refer to Table 8-3 for details.

9.3.7 Set fade Out Blinking (23h)

This command allows to set the fade mode and adjust the time interval for each fade step. Below figures show the example of Fade Out mode and Blinking mode.

Figure 9-3 : Example of Fade Out mode

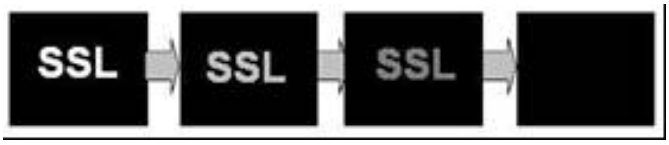


Figure 9-4 : Example of Blinking mode

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DDIO}	Supply Voltage	-0.3 to +6	V
V_{DD}		-0.3 to V_{DDIO}	V
V_{CC}		0 to 16	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than masimum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DDIO}). Unused outputs must be left open.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS},
V_{DDIO} = 2.4V to 3.6V,
T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-		8	-	15	V
V_{DDIO}	Low voltage power supply, power supply for I/O pins	Low Voltage I/O Application		2.4	-	3.6	V
		5V I/O Application		4.4	-	5.5	V
V_{DD}	Logic Supply Voltage	Low Voltage I/O Application		2.4	-	3.6	V
		5V I/O Application (V_{DD} as output)		-	-	-	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz		0.9 x V_{DDIO}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz		-	-	0.1 x V_{DDIO}	V
V_{IH}	High Logic Input Level	-		0.8 x V_{DDIO}	-	-	V
V_{IL}	Low Logic Input Level	-		-	-	0.2 x V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} = OFF V_{DD} (external: LV I/O mode) = 3.3V, Display OFF, No panel attached		-	-	10	uA
$I_{SLP\ VDDIO}$	V_{DDIO} Sleep mode Current	V_{DDIO} = 3.3V, V_{CC} =OFF Display OFF, No panel attached	Ext V_{DD} = 3.3V	-	-	10	uA
		V_{DDIO} = 5V, V_{CC} =OFF Display OFF, No panel attached	Enable Internal V_{DD} during Sleep mode (at 5V I/O mode)	-	55	70	uA
			Disable Internal V_{DD} during Sleep mode (Deep Sleep mode)	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CC} = 8~15V V_{DDIO} = 3.3V, V_{DD} (external) = 3.3V, or V_{DDIO} = 5V, V_{DD} (internal) Display OFF, No panel attached		-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DDIO} = V_{DD} = 3.3V, V_{CC} =12, Contrast = FFh, I_{REF} =15uA, No loading, Display ON, All ON			-	560	670	uA
I_{DDIO}	V_{DDIO} Supply Current V_{CC} = 12, Contrast = FFh, I_{REF} = 15uA , No loading, Display ON, All ON	V_{DDIO} = V_{DD} = 3.3V (Low Voltage I/O Application)		-	2	5	uA
		V_{DDIO} = 5V (Internal V_{DD}) (5V I/O Application)		-	130	160	uA

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{DD}	V_{DD} Supply Current $V_{DDIO} = V_{DD} = 3.3V$ (Low Voltage I/O Application), $V_{CC} = 12$, Contrast = FFh, $I_{REF} = 15uA$, No loading, Display ON, All ON		-	90	110	uA
I_{SEG}	Segment Output Current, $V_{DDIO} = V_{DD} = 3.3V$ (LV I/O) or $V_{DDIO} = 5V$ (5V I/O), $V_{CC} = 12V$, $I_{REF} = 15uA$, Display ON	Contrast=FFh	-	450	550	uA
		Contrast=AFh	-	340	-	
		Contrast=7Fh	-	225	-	
		Contrast=3Fh	-	112	-	
		Contrast=0Fh	-	56	-	
Dev	Segment output current uniformity	$Dev = (I_{SEG} - I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ $I_{SEG}[0:99]$ = Segment current at contrast setting = FFh	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

12 AC CHARACTERISTICS

12.1 AC Characteristics

Conditions:

Voltage referenced to V_{SS}

V_{DDIO} = 2.4 to 3.6V (Low Voltage I/O Application) or V_{DDIO} = 4.4V to 5.5V (5V I/O Application)

T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 3.3V or Internal V_{DD}	454	505	556	kHz
F_{FRM}	Frame Frequency for 32 MUX Mode	100x32 4-line Character Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1 / (D * K * 32)(2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	2000	-	-	ns

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

(2) D: Divide ratio

K: Phase 1 period + Phase 2 period + K_o , where K_o = 126

Default K is 18 + 7 + 126 = 151

12.2 6800-Series MCU Parallel Interface Timing Characteristics

Table 12-2: 6800-Series MCU Parallel Timing Characteristics

($TA = 25\ ^oC$, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note

(1) All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-1: 6800-series parallel interface characteristics (Form 1: CS# low pulse width > E high pulse width)

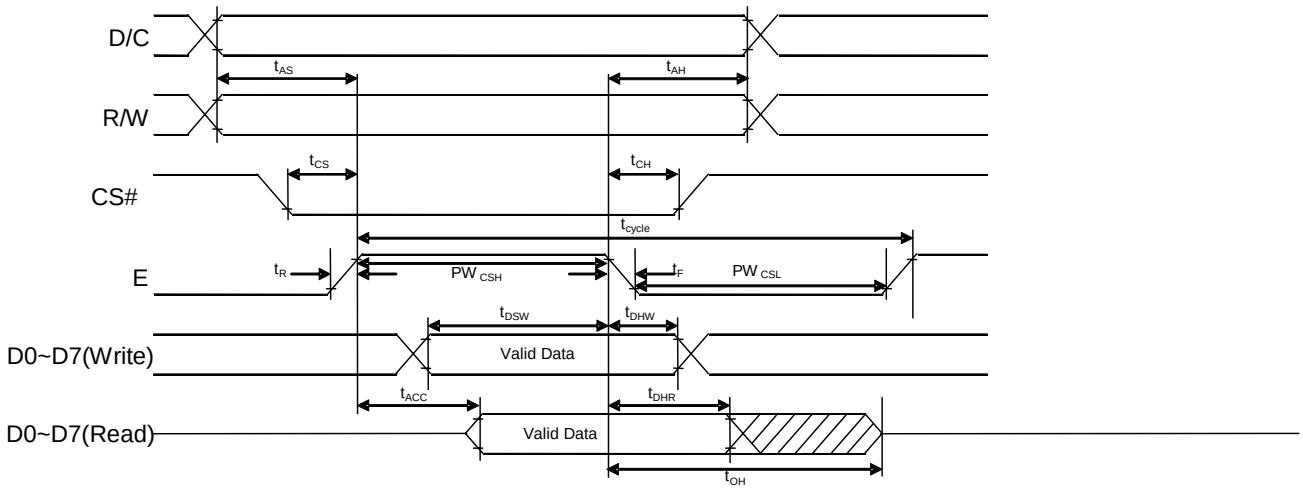
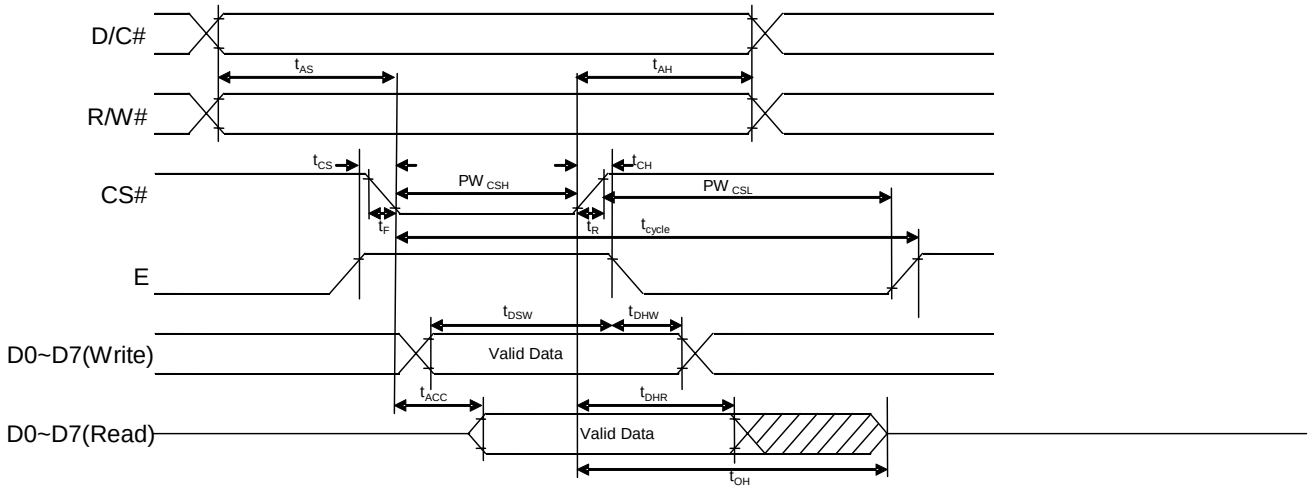


Figure 12-2: 6800-series parallel interface characteristics (Form 2: CS# low pulse width < E high pulse width)



12.3 8080-Series MCU Parallel Interface Timing Characteristics

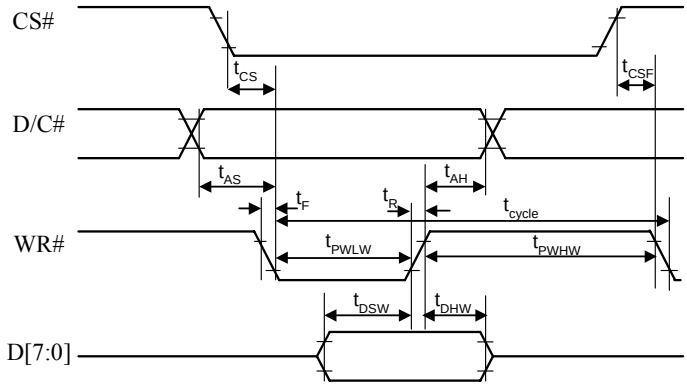
Table 12-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

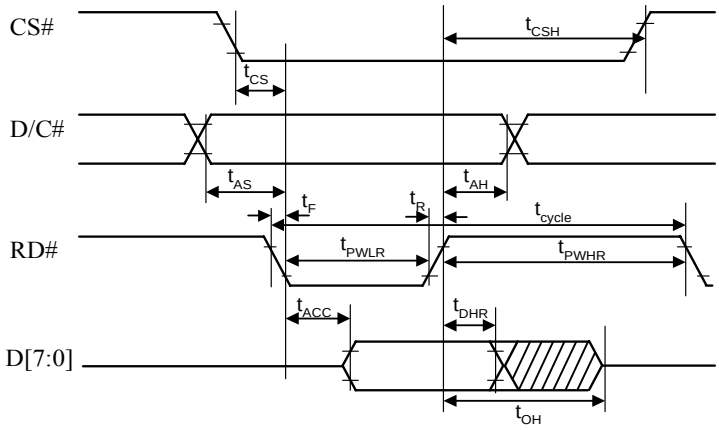
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	.0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-3 : 8080-series parallel interface characteristics

Write cycle



Read Cycle



12.4 Serial Interface Timing Characteristics

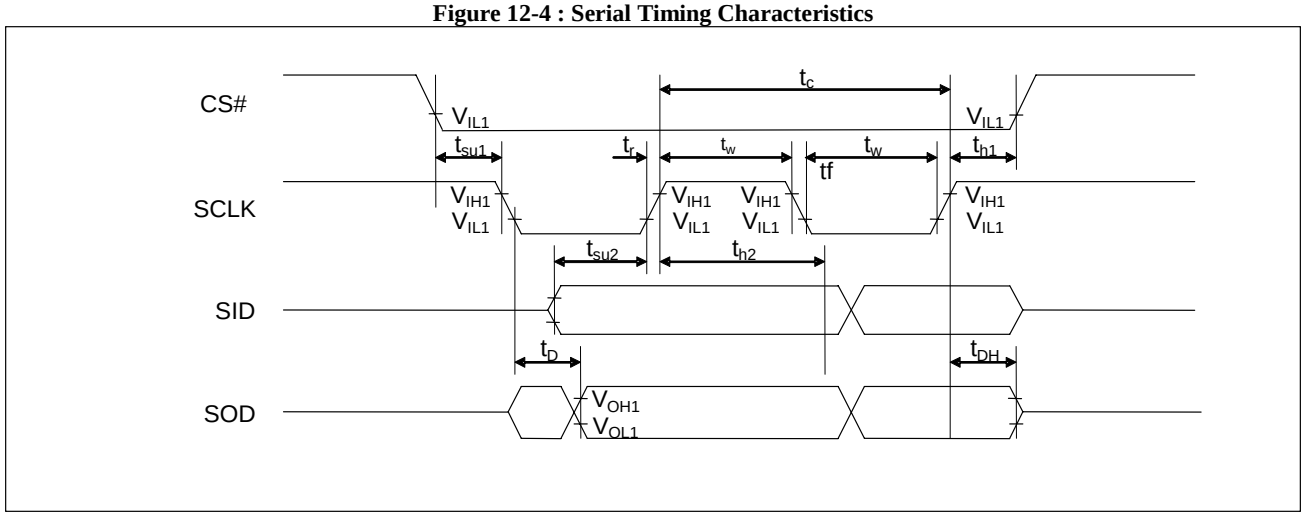
Table 12-4 : Serial Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	15	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	20	-	-	ns
t_D	Serial output data delay time	200	-	-	ns
t_{DH}	Serial output data hold time	10	-	-	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-4 : Serial Timing Characteristics



12.5 I²C Timing Characteristics

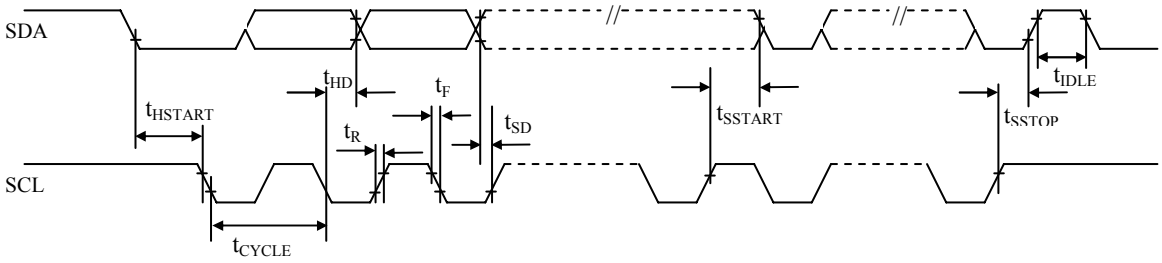
Table 12-5 : I²C Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	460	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

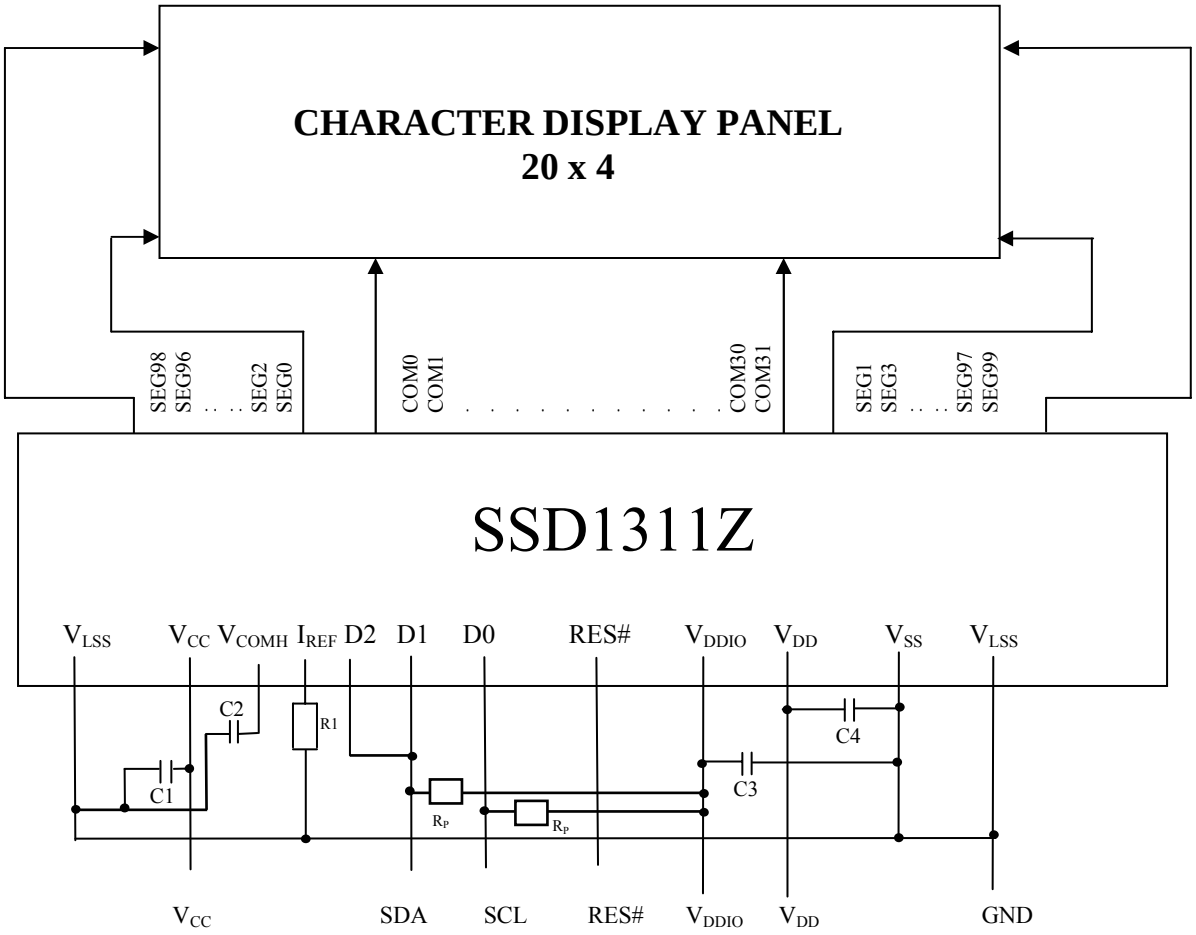
Figure 12-5 : I²C Timing Characteristics



13 APPLICATION EXAMPLE

Figure 13-1 : Application Example of SSD1311Z

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DDIO}=V_{DD}=3.3V, V_{CC} =12V, I_{REF}=15uA)



Pin connected to MCU interface: D[2:0], RES#
Pin internally connected to V_{SS}: D[7:3], BS0, BS2, E, R/W#, CS#, CL, OPR0, OPR1
Pin internally connected to V_{DD}: BS1, CLS, SHLC, SHLS, ROM0, ROM1
TR[9:0] should be left open.
D/C# acts as SA0 for slave address selection (3)

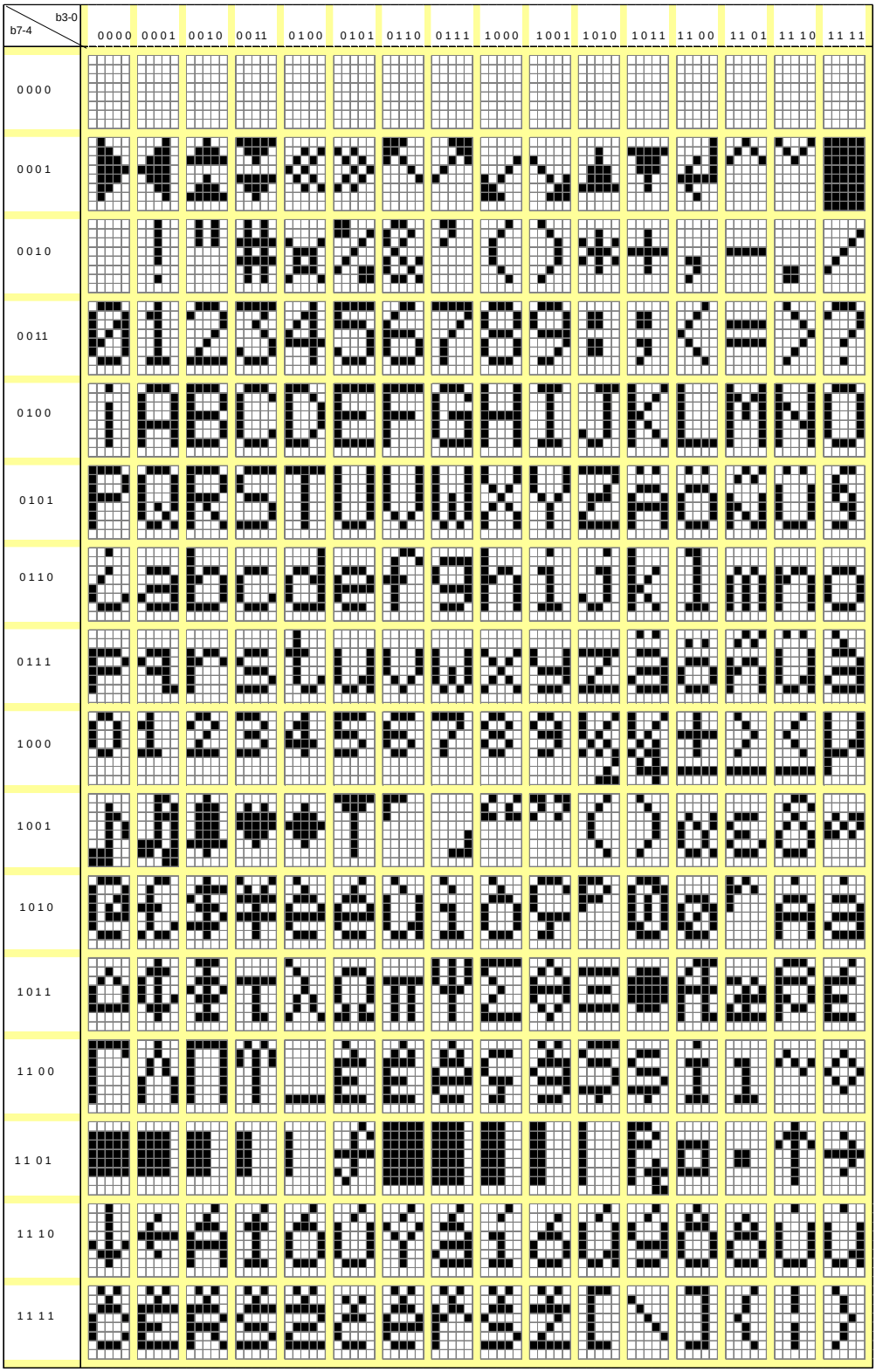
C1, C2: 4.7uF (1)
C3, C4: 1.0uF (1) place close to IC V_{DDIO} / V_{DD} and V_{SS} pins on PCB
R_P : Pull up resistor

Voltage at I_{REF} = V_{CC} – 4.5V. For V_{CC} = 12V, I_{REF} = 15uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
≈ (12-4.5)V / 15uA
= 500KΩ

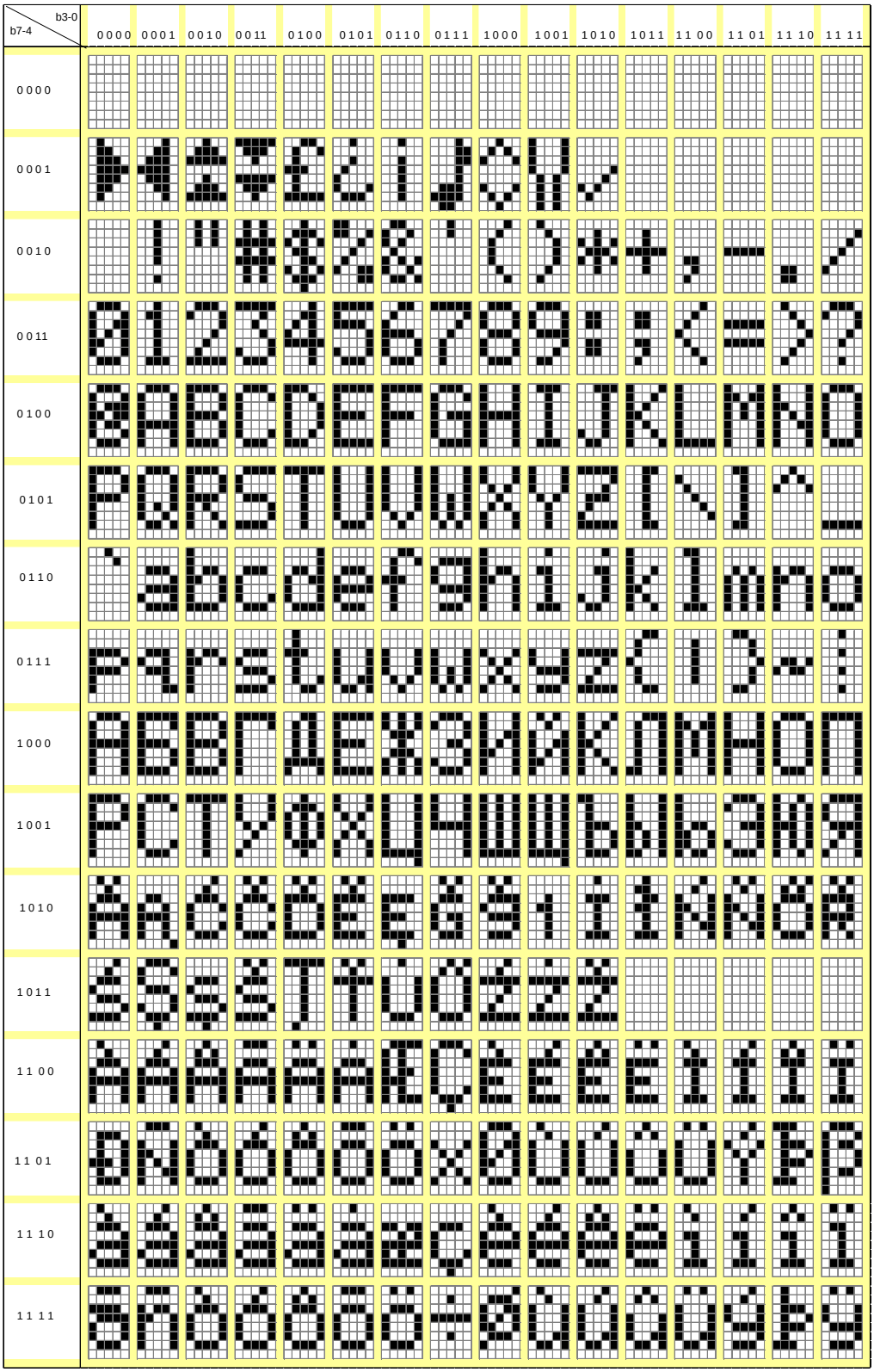
Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face down.
(3) Refer to Section 7.1.4 for details.
(4) It is recommended to tie V_{LSS} and V_{SS} at one common ground point to minimize circulating ground noise.

14 SSD1311 CGROM CHARACTER CODE

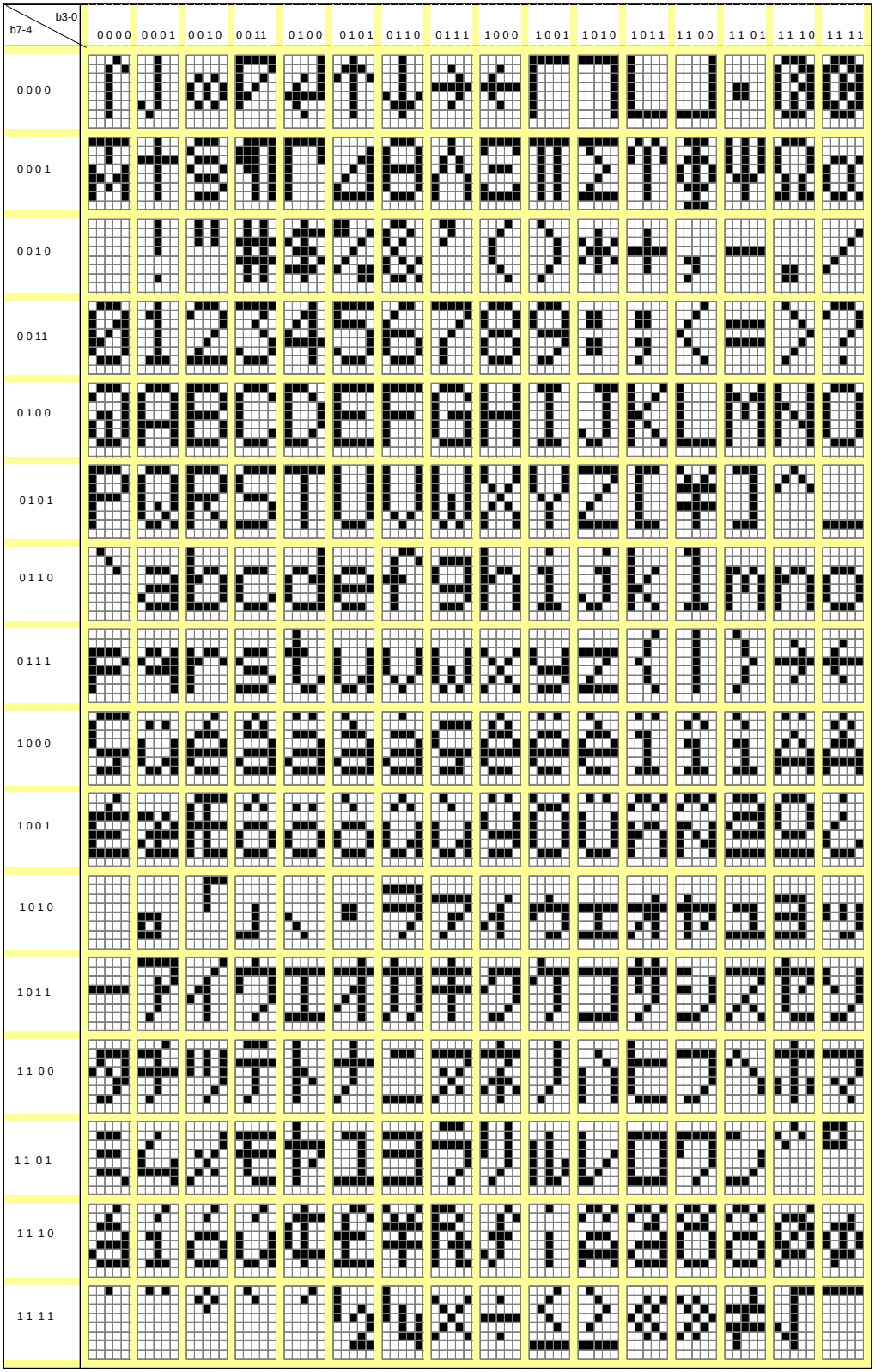
14.1 ROM A



14.2 ROM B


b3-0
b7-4
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111

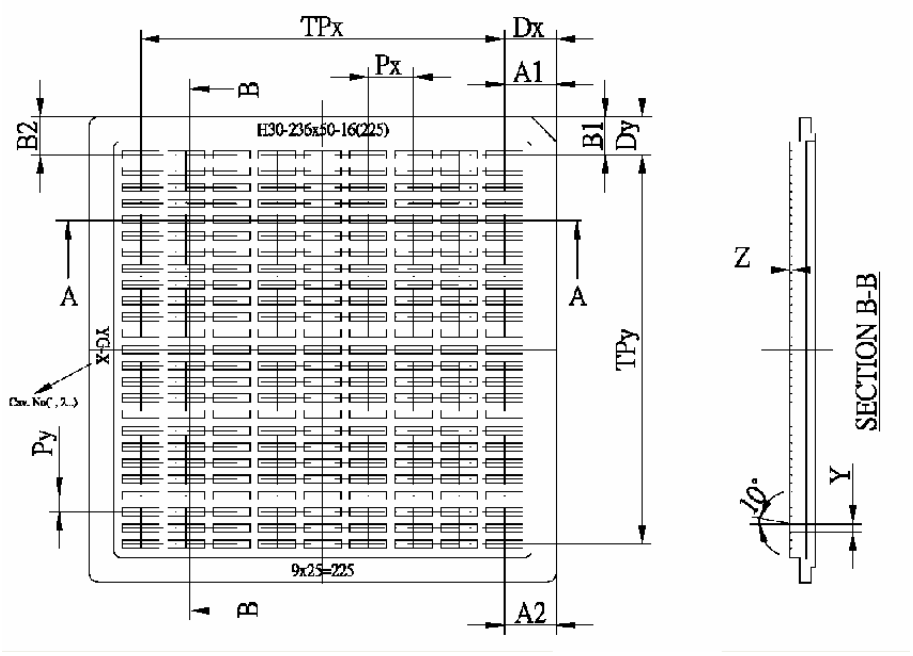
14.3 ROM C


b3-0
b7-4
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

15 PACKAGE INFORMATION

15.1 SSD1311M1Z Die Tray Information

Figure 15-1: SSD1311M1Z die tray information



Remarks:

1. Tray material: Permanent Antistatic
2. Tray color code: Black
3. Surface resistance $10^9 \sim 10^{12}\ \Omega$
4. Pocket bottom: Rough Surface

Parameter	Dimensions	
	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
D_X	8.40±0.10	(331)
TP_X	59.20±0.10	(2331)
D_Y	6.20±0.10	(244)
TP_Y	63.60±0.10	(2504)
P_X	7.40±0.05	(291)
P_Y	2.65±0.05	(104)
X	6.00±0.05	(236)
Y	1.27±0.05	(50)
Z	0.40±0.05	(16)
N (pocket number)	225	

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

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