SINO WEALTH

SH1111

32 X 100
OLED/PLED Driver with Controller
For 20*4 Characters and 32*100 Dot Matrix

PRELIMINARY

Features

- Single Chip PMOLED drivers
  - 32 Common drivers
  - 100 Segment drivers
- Maximum display dimensions
  - 16 characters * 1 lines
  - 20 characters * 1 lines
  - 20 characters * 2 lines
  - 40 characters * 1 lines (Cascade Application)
  - 40 characters * 2 lines (Cascade Application)
  - 16 characters * 4 lines
  - 20 characters * 4 lines
  - 100 * 32 dot matrix
- Support Graphic mode
- Support Cascade application
- Versatile display functions provided on chip:
  - Display Clear, Cursor Home, Display ON/OFF,
  - Cursor ON/OFF, Character Blinking, Cursor Shift
  - Display Shift
- Multiplexing duty factors, selected by register
  - Graphic mode: 1/1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8, 1/16, 1/32
  - Character mode: 1/8, 1/11, 1/16, 1/22, 1/32
- Character Displays Data RAM (DDRAM): 80 X 8 bits
- Graphic Displays Data RAM (GDDRAM): 100*32bits
- Character Generator RAM (CGRAM): 64 X 8 bits
  - 8 character (5*8 dot) or 4 character (5*10 dot)
- Supply 4 set Character Generator ROM (CGROM):
  - CGROM Size: 4 sets, 256 characters, 5*10 dot patterns
  - English Japanese Character
  - English Russian Character
  - Western European character-1
  - Western European character-2
- High speed 4/8-bit 6800, 8080 Parallel Interface, up to 2MHz
- 3-wire & 4-wire Serial Peripheral Interface
- 400KHz fast I^2C bus interface
- Maximum segment output current: 600μA
- Maximum common sink current: 60mA
- Build-in power on reset function
- Operating voltage:
  - Logic voltage supply: VDD1 = 2.2V - 3.5V or VDD1=3.5~5.5V (Pad option)
  - DC-DC voltage supply: VDD2 = 2.7V – 5.5V
- OLED Operating voltage supply:
  - External VPP supply = 5.0V - 14.0V
  - Internal Charge pump for VPP generator = 6.4V, 8.0V, 9.0V, 12.0V (select by register)
  - Programmable Internal Charge pump mode: 2 X VDD2 or 3 X VDD2 (select by register)
- Vertical scrolling in graphic mode
- Adjustable Pre-charge with register
- Adjustable Panel Brightness with 8 bit register
- Adjustable Cursor Blinking Duty with register
- Programmable frame frequency and multiplexing ratio
- On-chip oscillator
- Automatic Power On Reset Circuit
- Low power consumption
  - Sleep mode: < 10μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form, thickness: 300mm

General Description

SH1111 is an OLED Driver/Controller IC utilizing CMOS Technology specially designed to display alphanumeric and Japanese kana characters as well as symbols and graphics. It can interface with either 4/8 bit 6800-Parallel Interface, 4/8 bit 8080-Parallel Interface, 3/4 bit SPI Serial Interface and IIC Microprocessor and display up to one 20-character line, two 20-character lines, one 40-character lines, two 40-character lines, four 20-character lines or 100*32 dot matrix.

SH1111 embeds with contrast control, Display RAM oscillator, build-in Character Generator ROM and efficient DC-DC converter. Since all the functions such as Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, Display Shift are all incorporated into a single chip, a minimal system which having the highest performance and reliability can be interfaced with this OLED driver. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

Block Diagram

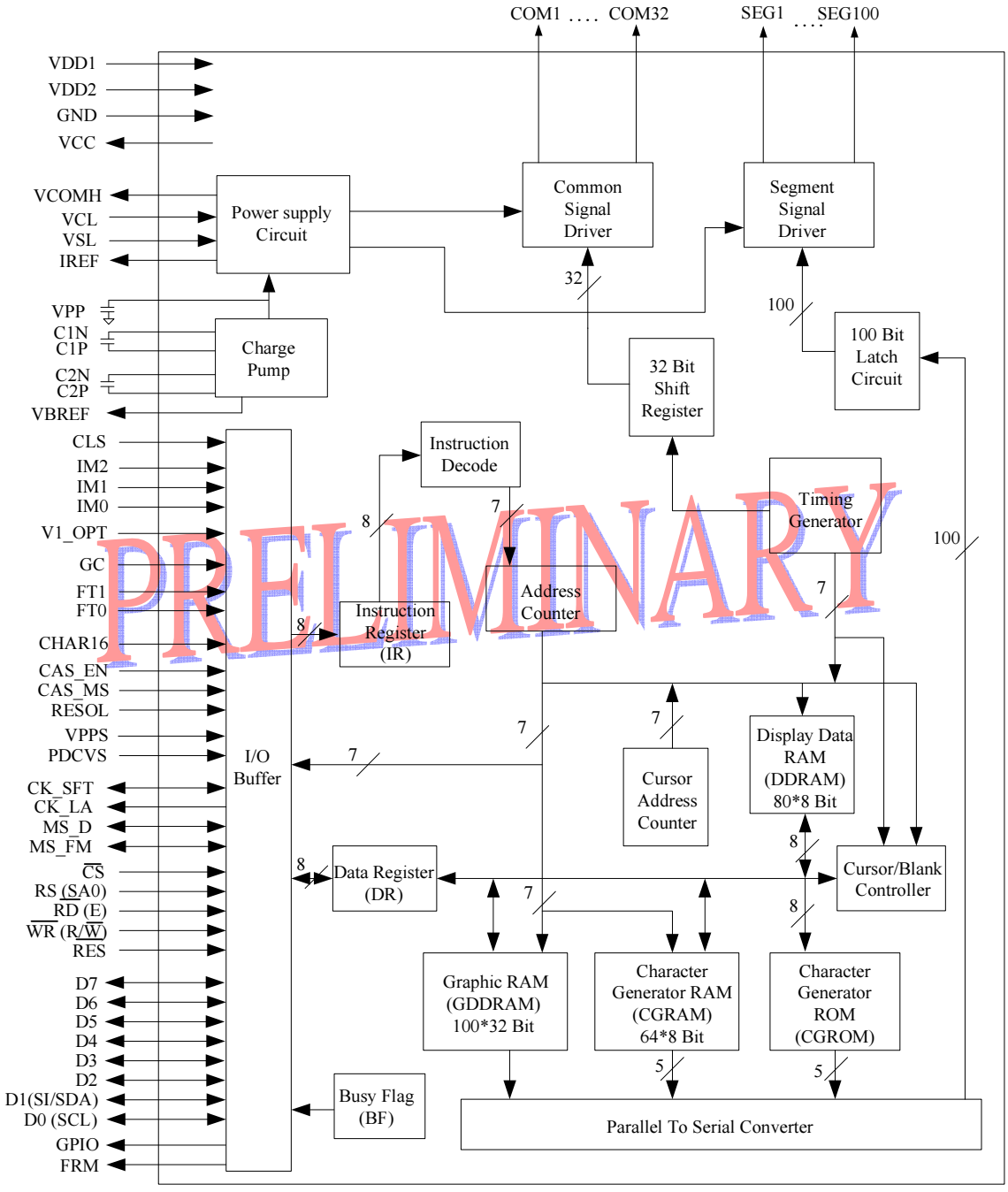


Figure.1 SH1111 Block Diagram

Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
44,45,46,53	V_{DD1}	Supply	2.2 ~ 3.5V or 3.5 ~ 5.5V power supply input pad for logic.
18,19,20,21	V_{DD2}	Supply	2.7 ~ 5.5V power supply pad for Power supply for charge pump circuit. This pin should be disconnected when VPP is supplied externally.
41,42,43	V_{CC}	O	Logic power output pad: When VDD1 = 2.2~3.5V, VCC output voltage VDD1. When VDD1 = 3.5~5.5V, VCC output voltage 2.8V. A capacitor should be connected between this pad and GND.
30~33,68,82,93	GND	Supply	Ground
38,39	V_{SL}	Supply	This is a segment voltage reference pad This pad should be connected to GND externally
34,35,36,37	V_{CL}	Supply	This is a common voltage reference pad This pad should be connected to GND externally

OLED Driver Supplies

Pad No.	Symbol	I/O	Description
22	I_{REF}	O	This is a segment current reference pad A resistor should be connected between this pad and GND. Set the current at 37.5μA
23,24,25	V_{COMH}	O	This is a pad for the voltage output high level for common signals A capacitor should be connected between this pad and GND
40	V_{BREF}	O	This is an internal voltage reference pad for booster circuit
26,27,28,29	V_{PP}	P	OLED panel power supply. Generated by internal charge pump.
2~5 6~9	C1N, C1P	P	Connect to charge pump capacitor. These pins are not used and should be disconnected when Vpp is supplied externally.
10~13 14~17	C2P, C2N	P	Connect to charge pump capacitor. These pins are not used and should be disconnected when Vpp is supplied externally.

System Pad Option Pads

Pad No.	Symbol	I/O	Description
54	CLS	I	This is the internal clock enable pad. In Master Mode CLS = "H": Internal oscillator circuit is enabled. CLS = "L": Internal oscillator circuit is disabled (requires external input). When CLS = "L", an external clock source must be connected to the CL pad for normal operation.
55 56 57	IM0 IM1 IM2	I	These are the MPU interface mode select pads.

IM2	IM1	IM0	MPU Interface
0	0	0	8-bit 6800
0	0	1	8-bit 8080
0	1	0	4-wire SPI
0	1	1	IIC
1	0	0	4-bit 6800
1	0	1	4-bit 8080
1	1	0	3-wire SPI
1	1	1	IIC

58	V1_OPT	I	This is the V1 supply voltage select pad. V1_OPT = "H": Power should supply "3.5~5.5V" to VDD1. V1_OPT = "L": Power should supply "2.2~3.5V" to VDD1.

<table>
<tr><td>59</td><td>GC</td><td>I</td><td>This bit is used to select the display mode for further process.
When G/C = “H”, the GRAPHIC MODE will be selected.
When G/C = “L”, the CHARACTER MODE will be selected.</td></tr>
<tr><td>60
61</td><td>FT0
FT1</td><td>I</td><td>Font Table Selection. These two bits are used to select one font table out of the four for further process.
<table>
<tr><th>FT1</th><th>FT0</th><th>Font Table</th></tr>
<tr><td>0</td><td>0</td><td>ENGLISH_JAPANESE CHARACTER FONT TABLE</td></tr>
<tr><td>0</td><td>1</td><td>WESTERN EUROPEAN CHARACTER FONT TABLE-I</td></tr>
<tr><td>1</td><td>0</td><td>ENGLISH_RUSSIAN CHARACTER FONT TABLE</td></tr>
<tr><td>1</td><td>1</td><td>WESTERN EUROPEAN CHARACTER FONT TABLE-II</td></tr>
</table></td></tr>
<tr><td>62</td><td>CAS_EN</td><td>I</td><td>Cascade Mode Open / Close:
CAS_EN = “H”, Cascade Mode Open. SH1111 is used as cascade mode, and the user can select SH1111 as Master or Slave.
CAS_EN = “L”, Cascade Mode Close, SH1111 is used as a single chip.</td></tr>
<tr><td>63</td><td>CAS_MS</td><td>I</td><td>SH1111 used as Master or Slave select pin:
CAS_MS = “H”, SH1111 used as Master Mode.
CAS_MS = “L”, SH1111 used as Slave Mode.</td></tr>
<tr><td>64</td><td>RESOL</td><td>I</td><td>Display Resolution Mode Select:
RESOL = “H”, the display resolution of SH1111 is 20 characters * 4 line (COM output 1/32 duty).
RESOL = “L”, the display resolution of SH1111 is 20 characters * 2 line (COM output 1/16 duty).</td></tr>
<tr><td>65</td><td>VPPS</td><td>I</td><td>This Pad is used to control internal pump open or close.
VPPS = “H”, Internal Charge pump for VPP generator open, user can use internal charge pump to generate VPP.
VPPS = “L”, Internal Charge pump for VPP generator close, requires external VPP.</td></tr>
<tr><td>66</td><td>CHAR16</td><td>I</td><td>This Pad is used to select the special application 16 character * 1 line and 16 character * 4 line.
CHAR16 = 0, special application 16 character *1 line and 16 character * 4 line disable.
CHAR16 = 1, special application 16 character *1 line and 16 character * 4 line enable.
<table>
<tr><th>CHAR16</th><th>RESOL</th><th>Display Dimensions</th><th>SEG</th></tr>
<tr><td>0</td><td>*</td><td>Normal Display</td><td>SEG1~SEG100</td></tr>
<tr><td>1</td><td>0</td><td>16 character × 1 line</td><td>SEG1~SEG80</td></tr>
<tr><td>1</td><td>1</td><td>16 character × 4 line</td><td>SEG1~SEG80</td></tr>
</table></td></tr>
<tr><td>67</td><td>PDCVS</td><td>I</td><td>This pad is used to set the default value of Pre-Charge/Dis-Charge, Contrast, VCOMH.
<table>
<tr><th>PVDS Value</th><th>Parameters</th><th>Default value</th><th>Parameter</th></tr>
<tr><td rowspan="4">PDCVS = “H”</td><td>Pre-Charge</td><td>FH</td><td>15DCLKS</td></tr>
<tr><td>Dis-Charge</td><td>FH</td><td>15DCLKS</td></tr>
<tr><td>Contrast</td><td>FFH</td><td></td></tr>
<tr><td>VCOMH</td><td>40H</td><td>VPP</td></tr>
<tr><td rowspan="4">PDCVS = “L”</td><td>Pre-Charge</td><td>2H</td><td>2DCLKS</td></tr>
<tr><td>Dis-Charge</td><td>2H</td><td>2DCLKS</td></tr>
<tr><td>Contrast</td><td>80H</td><td></td></tr>
<tr><td>VCOMH</td><td>35H</td><td>0.770×VPP</td></tr>
</table></td></tr>
</table>

System Bus Connection Pads

Pad No.	Symbol	I/O	Description
50	CL	I/O	This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.
69,70,71	CK_SFT	I/O	Character pattern data shift clock , only used in cascade application When "Master" mode, CK_SFT is output When "slave" mode, CK_SFT is input When the chip is used in single mode, CK_SFT must be floating.
72,73	CK_LA	O	CK_LA output GND.
74,75,76	MS_D	I/O	Character Pattern Data Pin, only used in cascade application When "master" mode, MS_D is output When "slave" mode, MS_D is input When the chip is used in single mode, MS_D must be floating.
77,78	MS_FM	I/O	Master/Slaver connect for synchronism, only used in cascade application When "master" mode, MS_FM is output When "slave" mode, MS_FM is input When the chip is used in single mode, MS_FM output GND. MS_FM must be floating.
79	$\overline{CS}$	I	This pad is the chip select input. When $\overline{CS}$ = "L", then the chip select becomes active, and data/command I/O is enabled.
80	$\overline{RES}$	I	This is a reset signal input pad. When $\overline{RES}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.
81	RS	I	This is the Data/Command control pad that determines whether the data bits are data or a command. RS = "H": the inputs at D0 to D7 are treated as display data. RS = "L": the inputs at D0 to D7 are transferred to the command registers. In IIC interface, this pad serves as SA0 to distinguish the different address of OLED driver.
83	$\overline{WR}$ (R/$\overline{W}$)	I	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ = "H": Read. When R/$\overline{W}$ = "L": Write.
84	$\overline{RD}$ (E)	I	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the SH1111 data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
85 86 87,88 89~92	D0(SCL) D1(SI/SDA) D2– D3 D4 – D7	I/O	When 8-bit bus mode, D0-D7 are used as bi-directional data bus that connects to an 8-bit MPU data bus. When 4-bit bus mode, D4-D7 are used as bi-directional data bus that connects to a 4-bit MPU data bus. And in this case D0-D3 pins are not used and set to HZ. When the serial interface is select, then D1 serves as the serial data input terminal (SI/SDA) and D0 serves as the serial clock input terminal (SCL). At this time, D7 to D2 are set to HZ. When the chip select is inactive, D0 to D7 are set to HZ.
51	FRM	O	This pad is No Connection pad. Its signal varies with the frame frequency. Its voltage is equal to VDD1 when the last common output of every frame is active, and is equal to GND during other time.

52	GPIO	O	This pad is used to indicate the Display ON/OFF status. When Display On, this pad output voltage VDD1. When Display Off, this pad output voltage GND.

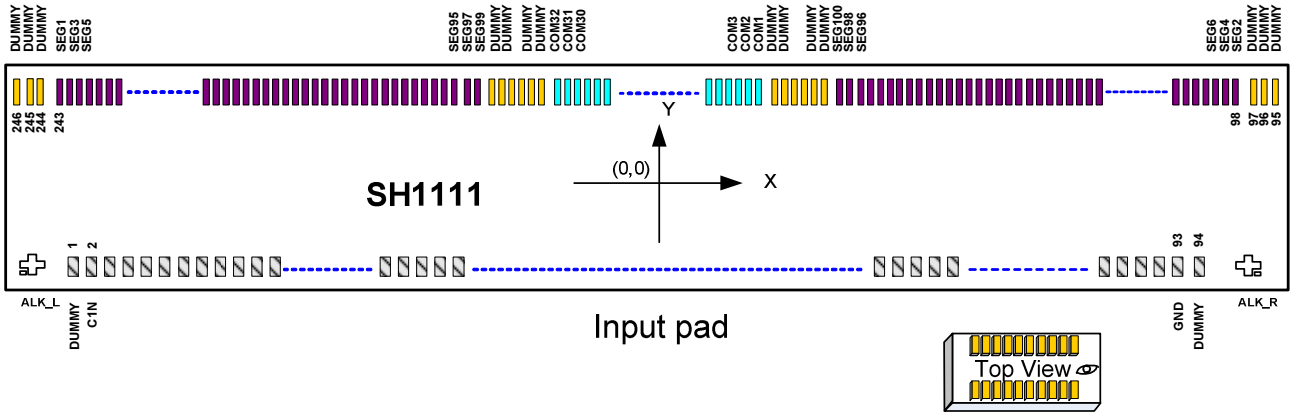
OLED Drive Pads

Pad No.	Symbol	I/O	Description
154~169,172~187	COM1 - 32	O	These pads are Common signal output for OLED display.
98~147,194~243	SEG1 - 100	O	These pads are Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
47	Test1	O	Test pads, internal pull low, no connection for user.
48	Test2	O	Test pads, no connection for user.
49	Test3	O	Test pads, no connection for user.
1,94~97,148~153, 170~171,188~193 244~246	Dummy	-	Dummy pads, no connection for user.

Pad Configuration



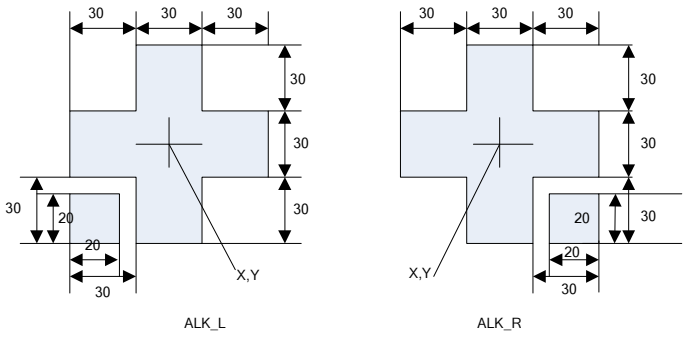
Chip Outline Dimensions

Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	5444	868
Chip height	All pads	300	
Bump size	I/O	40	80
	SEG	15	110
	COM	15	110
Pad pitch	COM	46	
	SEG	30.75	
	I/O	55	
Bump height	All pads	9±2	

Alignment Mark Location

unit: μm

NO	X	Y
ALK_L	-2616.01	220
ALK_R	2616.01	220



Pad location (Total : 242 pads)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY	-2600.5	-353	69	CK_SFT	1225.5	-353	137	SEG80	1342.75	335	205	SEG77	-1373.5	335
2	C1N	-2545.5	-353	70	CK_SFT	1280.5	-353	138	SEG82	1312	335	206	SEG75	-1404.25	335
3	C1N	-2490.5	-353	71	CK_SFT	1335.5	-353	139	SEG84	1281.25	335	207	SEG73	-1435	335
4	C1N	-2435.5	-353	72	CK_LA	1390.5	-353	140	SEG86	1250.5	335	208	SEG71	-1465.75	335
5	C1N	-2380.5	-353	73	CK_LA	1445.5	-353	141	SEG88	1219.75	335	209	SEG69	-1496.5	335
6	C1P	-2325.5	-353	74	MS_D	1500.5	-353	142	SEG90	1189	335	210	SEG67	-1527.25	335
7	C1P	-2270.5	-353	75	MS_D	1555.5	-353	143	SEG92	1158.25	335	211	SEG65	-1558	335
8	C1P	-2215.5	-353	76	MS_D	1610.5	-353	144	SEG94	1127.5	335	212	SEG63	-1588.75	335
9	C1P	-2160.5	-353	77	MS_FM	1665.5	-353	145	SEG96	1096.75	335	213	SEG61	-1619.5	335
10	C2P	-2105.5	-353	78	MS_FM	1720.5	-353	146	SEG98	1066	335	214	SEG59	-1650.25	335
11	C2P	-2050.5	-353	79	CSB	1775.5	-353	147	SEG100	1035.25	335	215	SEG57	-1681	335
12	C2P	-1995.5	-353	80	RESB	1830.5	-353	148	DUMMY	1004.5	335	216	SEG55	-1711.75	335
13	C2P	-1940.5	-353	81	RS	1885.5	-353	149	DUMMY	973.75	335	217	SEG53	-1742.5	335
14	C2N	-1885.5	-353	82	GND	1940.5	-353	150	DUMMY	943	335	218	SEG51	-1773.25	335
15	C2N	-1830.5	-353	83	WRB	1995.5	-353	151	DUMMY	897	335	219	SEG49	-1804	335
16	C2N	-1775.5	-353	84	RDB	2050.5	-353	152	DUMMY	851	335	220	SEG47	-1834.75	335
17	C2N	-1720.5	-353	85	D0	2105.5	-353	153	DUMMY	805	335	221	SEG45	-1865.5	335
18	VDD2	-1665.5	-353	86	D1	2160.5	-353	154	COM1	759	335	222	SEG43	-1896.25	335
19	VDD2	-1610.5	-353	87	D2	2215.5	-353	155	COM2	713	335	223	SEG41	-1927	335
20	VDD2	-1555.5	-353	88	D3	2270.5	-353	156	COM3	667	335	224	SEG39	-1957.75	335
21	VDD2	-1500.5	-353	89	D4	2325.5	-353	157	COM4	621	335	225	SEG37	-1988.5	335
22	IREF	-1445.5	-353	90	D5	2380.5	-353	158	COM5	575	335	226	SEG35	-2019.25	335
23	VCOMH	-1390.5	-353	91	D6	2435.5	-353	159	COM6	529	335	227	SEG33	-2050	335
24	VCOMH	-1335.5	-353	92	D7	2490.5	-353	160	COM7	483	335	228	SEG31	-2080.75	335
25	VCOMH	-1280.5	-353	93	GND	2545.5	-353	161	COM8	437	335	229	SEG29	-2111.5	335
26	VPP	-1225.5	-353	94	DUMMY	2600.5	-353	162	COM9	391	335	230	SEG27	-2142.25	335
27	VPP	-1170.5	-353	95	DUMMY	2634.25	335	163	COM10	345	335	231	SEG25	-2173	335
28	VPP	-1115.5	-353	96	DUMMY	2603.5	335	164	COM11	299	335	232	SEG23	-2203.75	335
29	VPP	-1060.5	-353	97	DUMMY	2572.75	335	165	COM12	253	335	233	SEG21	-2234.5	335
30	GND	-1005.5	-353	98	SEG2	2542	335	166	COM13	207	335	234	SEG19	-2265.25	335
31	GND	-950.5	-353	99	SEG4	2511.25	335	167	COM14	161	335	235	SEG17	-2296	335
32	GND	-895.5	-353	100	SEG6	2480.5	335	168	COM15	115	335	236	SEG15	-2326.75	335
33	GND	-840.5	-353	101	SEG8	2449.75	335	169	COM16	69	335	237	SEG13	-2357.5	335
34	VCL	-785.5	-353	102	SEG10	2419	335	170	DUMMY	23	335	238	SEG11	-2388.25	335
35	VCL	-730.5	-353	103	SEG12	2388.25	335	171	DUMMY	-23	335	239	SEG9	-2419	335
36	VCL	-675.5	-353	104	SEG14	2357.5	335	172	COM17	-69	335	240	SEG7	-2449.75	335
37	VCL	-620.5	-353	105	SEG16	2326.75	335	173	COM18	-115	335	241	SEG5	-2480.5	335
38	VSL	-565.5	-353	106	SEG18	2296	335	174	COM19	-161	335	242	SEG3	-2511.25	335
39	VSL	-510.5	-353	107	SEG20	2265.25	335	175	COM20	-207	335	243	SEG1	-2542	335
40	VBREF	-455.5	-353	108	SEG22	2234.5	335	176	COM21	-253	335	244	DUMMY	-2572.75	335
41	VCC	-400.5	-353	109	SEG24	2203.75	335	177	COM22	-299	335	245	DUMMY	-2603.5	335
42	VCC	-345.5	-353	110	SEG26	2173	335	178	COM23	-345	335	246	DUMMY	-2634.25	335
43	VCC	-290.5	-353	111	SEG28	2142.25	335	179	COM24	-391	335				
44	VDD1	-235.5	-353	112	SEG30	2111.5	335	180	COM25	-437	335				
45	VDD1	-180.5	-353	113	SEG32	2080.75	335	181	COM26	-483	335				
46	VDD1	-125.5	-353	114	SEG34	2050	335	182	COM27	-529	335				
47	TEST1	-70.5	-353	115	SEG36	2019.25	335	183	COM28	-575	335				
48	TEST2	70.5	-353	116	SEG38	1988.5	335	184	COM29	-621	335				
49	TEST3	125.5	-353	117	SEG40	1957.75	335	185	COM30	-667	335				
50	CL	180.5	-353	118	SEG42	1927	335	186	COM31	-713	335				
51	FRM	235.5	-353	119	SEG44	1896.25	335	187	COM32	-759	335				
52	GPIO	290.5	-353	120	SEG46	1865.5	335	188	DUMMY	-805	335				
53	VDD1	345.5	-353	121	SEG48	1834.75	335	189	DUMMY	-851	335				
54	CLS	400.5	-353	122	SEG50	1804	335	190	DUMMY	-897	335				
55	IM0	455.5	-353	123	SEG52	1773.25	335	191	DUMMY	-943	335				
56	IM1	510.5	-353	124	SEG54	1742.5	335	192	DUMMY	-973.75	335				
57	IM2	565.5	-353	125	SEG56	1711.75	335	193	DUMMY	-1004.5	335				
58	V1_OPT	620.5	-353	126	SEG58	1681	335	194	SEG99	-1035.25	335				
59	GC	675.5	-353	127	SEG60	1650.25	335	195	SEG97	-1066	335				
60	FT0	730.5	-353	128	SEG62	1619.5	335	196	SEG95	-1096.75	335				
61	FT1	785.5	-353	129	SEG64	1588.75	335	197	SEG93	-1127.5	335				
62	CAS_EN	840.5	-353	130	SEG66	1558	335	198	SEG91	-1158.25	335				
63	CAS_MS	895.5	-353	131	SEG68	1527.25	335	199	SEG89	-1189	335				
64	RESOL	950.5	-353	132	SEG70	1496.5	335	200	SEG87	-1219.75	335				
65	VPPS	1005.5	-353	133	SEG72	1465.75	335	201	SEG85	-1250.5	335				
66	CHAR16	1060.5	-353	134	SEG74	1435	335	202	SEG83	-1281.25	335				
67	PDCVS	1115.5	-353	135	SEG76	1404.25	335	203	SEG81	-1312	335				
68	GND	1170.5	-353	136	SEG78	1373.5	335	204	SEG79	-1342.75	335				

Functional Description

Microprocessor Interface Selection

The 4/8 bit 8080-Parallel Interface, 4/8 bit 6800-Parallel Interface, 3-wire Serial Interface (SPI), 4-wire Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM2~0 as shown in Table 1.

Table. 1

				Data signal								Control signal				
IM2	**IM1**	**IM0**	**Interface**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E/$\overline{RD}$**	**$\overline{WR}$**	**$\overline{CS}$**	**RS**	**$\overline{RES}$**
0	0	0	8-bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	RS	$\overline{RES}$
0	0	1	8-bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	RS	$\overline{RES}$
0	1	0	4-wire SPI	Hz(Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	RS	$\overline{RES}$
0	1	1	IIC	Hz(Note1)						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$
1	0	0	4-bit 6800	D7	D6	D5	D4	Hz(Note2)				E	R/$\overline{W}$	$\overline{CS}$	RS	$\overline{RES}$
1	0	1	4-bit 8080	D7	D6	D5	D4	Hz(Note2)				$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	RS	$\overline{RES}$
1	1	0	3-wire SPI	Hz(Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	Pull Low	$\overline{RES}$
1	1	1	IIC	Hz(Note1)						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$

Note1: When 3-wire Serial Interface (SPI), 4-wire Serial Interface (SPI) or IIC Interface is selected, D7~D2 is Hz. D7~ D2 is recommended to connect the VDD1 or GND. It is also allowed to leave D7~ D2 unconnected.
Note2: When 4/8 bit 6800-Parallel Interface or 4/8 bit 8080-Parallel Interface is selected, D3~D0 is Hz. D3~ D0 is recommended to connect the VDD1 or GND. It is also allowed to leave D3~ D0 unconnected.

8bit 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), RS and $\overline{CS}$. When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table. .

Table. 2

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D0
0	0	0	8 bit 6800 microprocessor bus	$\overline{CS}$	RS	E	R/$\overline{W}$	D7 to D0

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. Below.

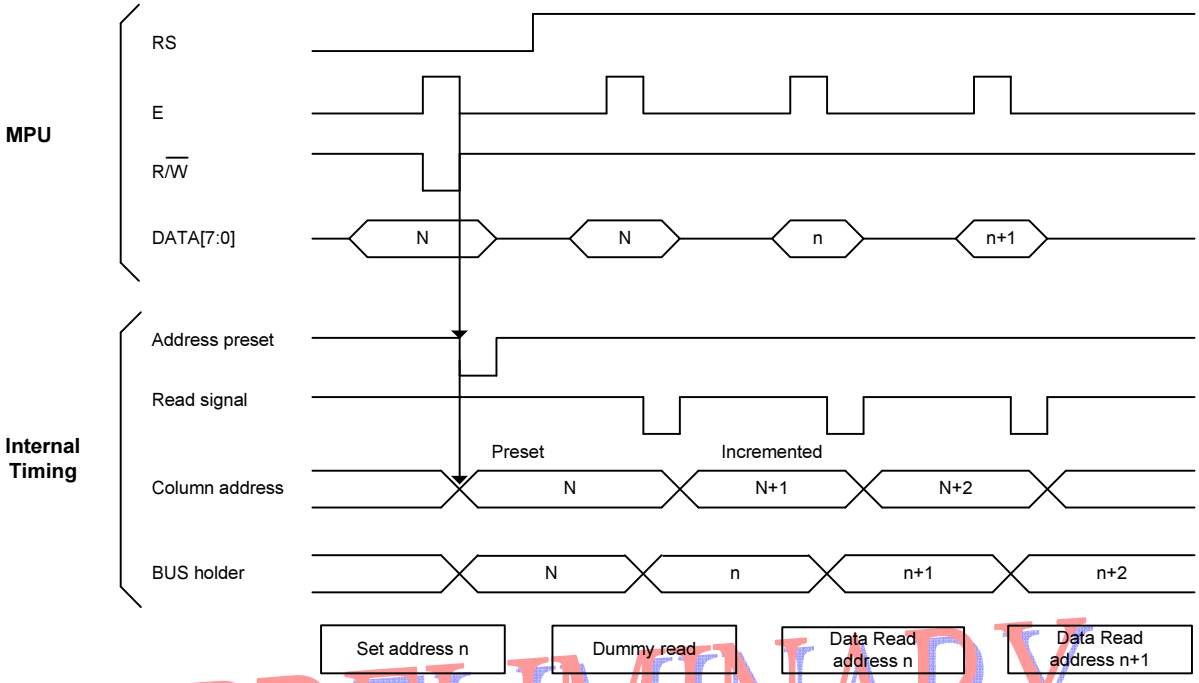


Figure.2

4bit 6800-series Parallel Interface

The parallel interface consists of 4 bi-directional data pads (D7~D4), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), RS and $\overline{CS}$ (D3~D0: HZ). When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of RS input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table.

Table. 3

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D4	D3 to D0
1	0	0	4bit 6800 microprocessor bus	$\overline{CS}$	RS	E	R/$\overline{W}$	D7 to D4	HZ

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. Below.

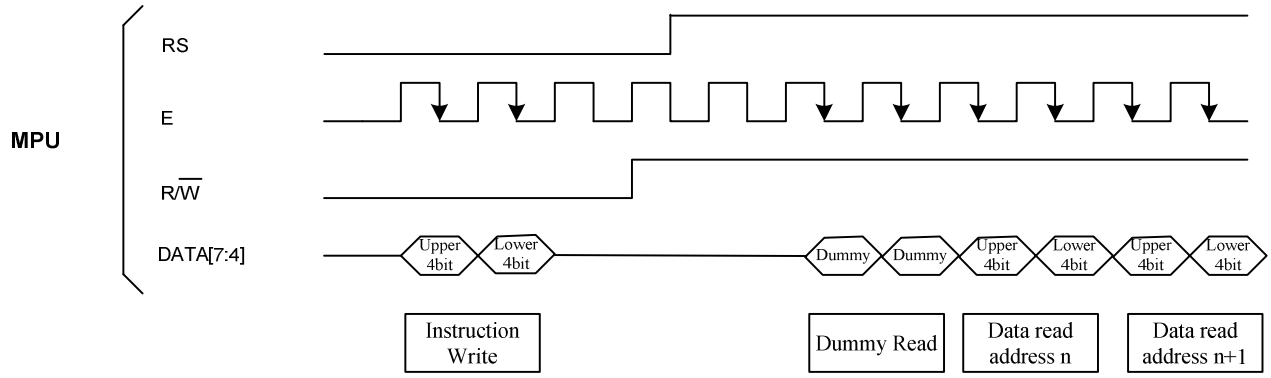


Figure.3

8bit 8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), RS and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by RS signal. The $\overline{WR}$ (R/$\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table. .

Table. 4

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D0
0	0	1	8 bit 8080 microprocessor bus	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D0

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1111 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals.

Table. 5

Common	4/8 bit 6800 processor	4/8 bit 8080 processor		Function
RS	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

4bit 8080-series Parallel Interface

The parallel interface consists of 4 bi-directional data pads (D7~D4), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), RS and $\overline{CS}$ (D3~D0: HZ). The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by RS signal. The $\overline{WR}$ (R/$\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table. .

Table. 6

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D4	D3 to D0
1	0	1	4 bit 8080 microprocessor bus	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D4	HZ

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, RS and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure.

Table. 7

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D2	D1	D0
0	1	0	4-wire SPI	$\overline{CS}$	RS	-	-	(HZ)	SI	SCL

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or GND. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

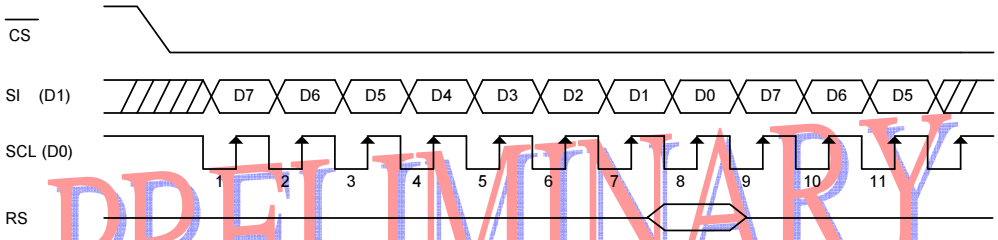


Figure.4 4-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into an 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6, … and D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0). See Figure 4.

Table. 8

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D2	D1	D0
1	0	1	3-wire SPI	$\overline{CS}$	Pull Low	-	-	(HZ)	SI	SCL

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or GND. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

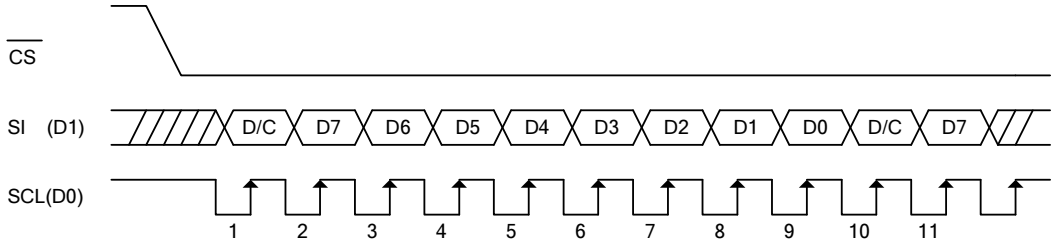


Figure.5 3-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I²C-bus Interface

The SH1111 can transfer data via a standard I²C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

Table. 9

IM2	IM1	IM0	Type	$\overline{CS}$	RS	$\overline{RD}$	$\overline{WR}$	D7 to D0	D1	D0
0	1	1	I²C Interface	Pull Low	SA0	-	-	(HZ)	SDA	SCL

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD1} or GND. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ signal could always pull low in I²C-bus application.

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different Ics or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

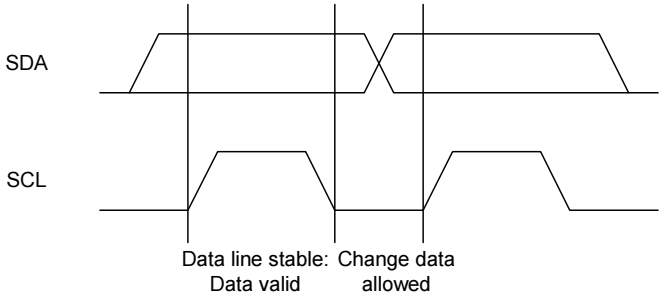


Figure.6 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

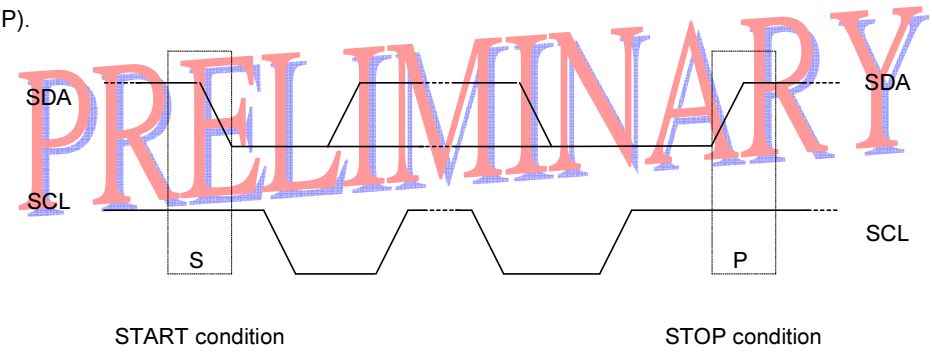


Figure.7 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

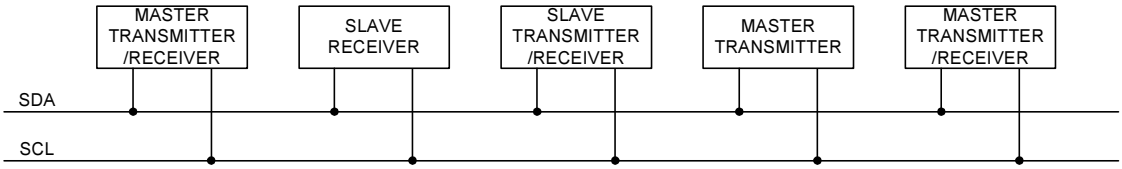


Figure.8 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

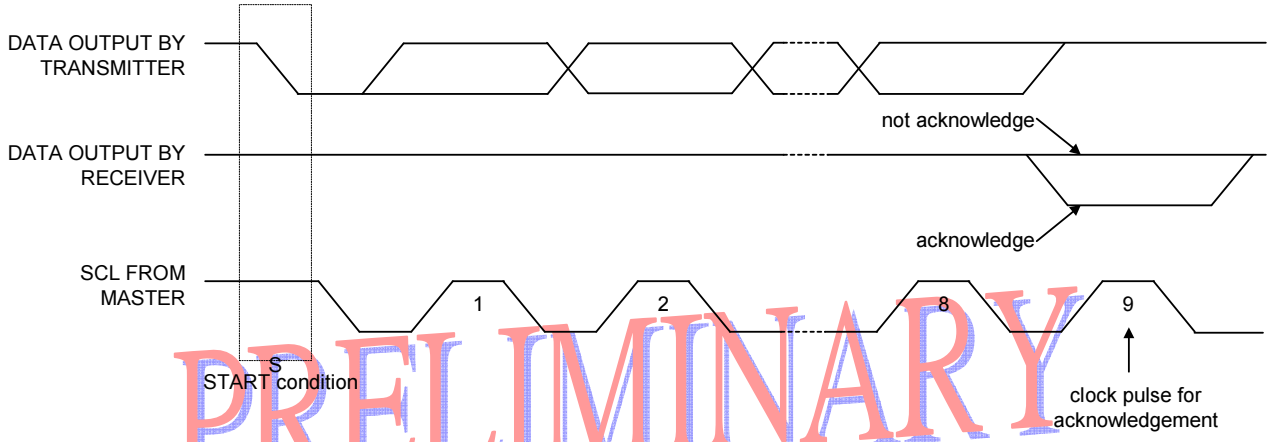


Figure.9 Acknowledge

Protocol

The SH1111 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^2C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1111. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1 (VDD1). The I^2C-bus protocol is illustrated in Fig.9. The sequence is initiated with a START condition (S) from the I^2C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$ (note1), plus a data byte (see Fig.7). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1111 device. If the D/$\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^2C-bus master issues a stop condition (P). If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

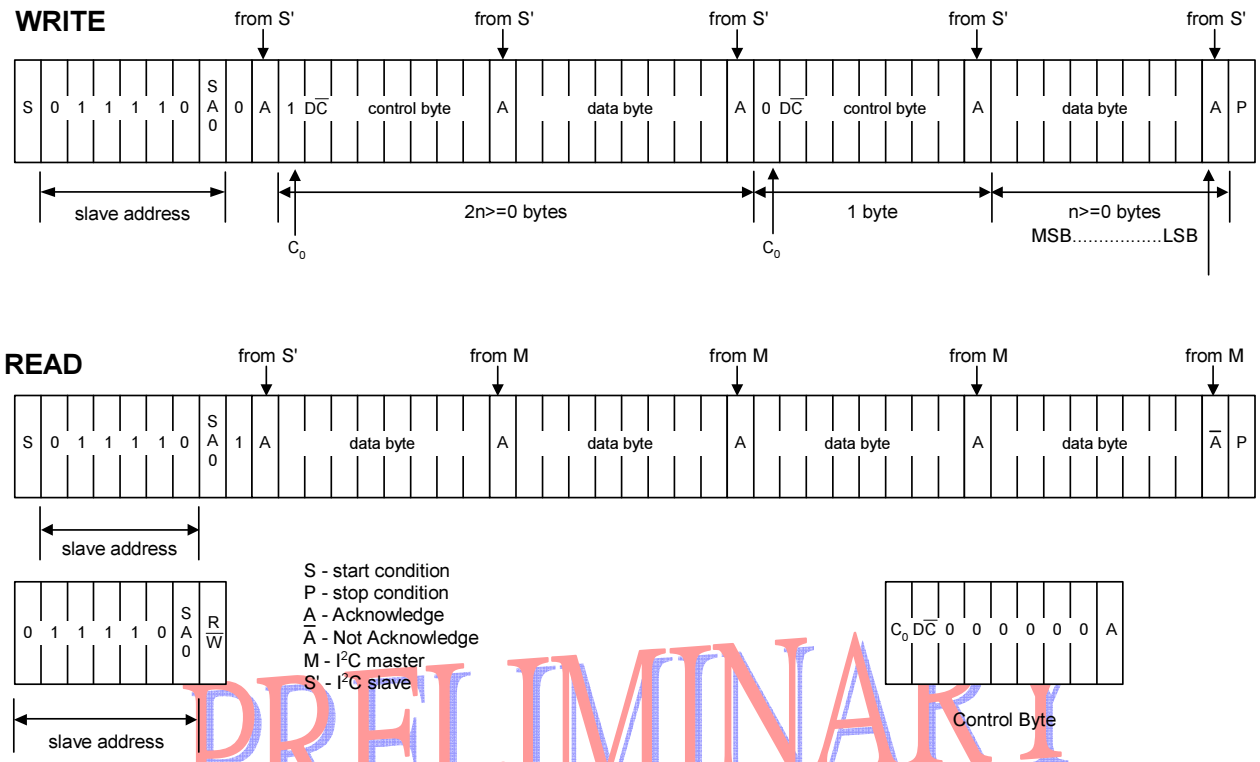


Figure.10 I²C Protocol

Note1:

1. Co= "0" : The last control byte , only data bytes to follow,
   Co= "1" : Next two bytes are a data byte and another control byte;
2. D/$\overline{C}$ = "0" : The data byte is for command operation,
   D/$\overline{C}$ = "1" : The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When RS = "H", the inputs at D7 – D0 are interpreted as data and be written to display RAM. When RS = "L", the inputs at D7 – D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Address Counter (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins – DB0 to DB6.

Character Mode Addressing——Display Data RAM (DDRAM)

SH1111 provides two kind of character mode. Character mode address can be controlled by DDRAM address instruction.

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 80 x 8-bits or 80 characters.

The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			Low Order Bits			
Address Counter(hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Case1: 1-Line Display(5×8 dot Font)

When the number of characters displayed is less than 80, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position(Digit)	1	2	3	4	·····	37	38	39	40	41	42	43	44	·····	77	78	79	80
DDRAM Address(hex)	00	01	02	03	·····	24	25	26	27	28	29	2A	2B	·····	4C	4D	4E	4F

(a) 8 characters x 1 line Case(5×8 dot Font, 5×10 dot Font): When only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8
DDRAM Address(hex)	00	01	02	03	04	05	06	07
Shift Left	01	02	03	04	05	06	07	08
Shift Right	4F	00	01	02	03	04	05	06

(b) 16 characters x l line (When N=1, 5×8 dot Font): When 16 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below. (Special Application 16 characters* 1 line, 5*8 Font only)

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address(hex)	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47
Shift Left	01	02	03	04	05	06	07	08	41	42	43	44	45	46	47	48
Shift Right	27	00	01	02	03	04	05	06	67	40	41	42	43	44	45	46

Note:

<1>Display Position 1~8 DDRAM: 00H~27H, the first address is 00H. Shift Right：00H → 27H → 26H → 25H …… 04H → 03H → 02H → 01H → 00H → 27H.

<2>Display Position 9~16 DDRAM: 40H~67H, the first address is 40H. Shift Right: 40H → 67H → 68H → 67H ……→44H → 43H → 42H → 41H → 40H →67H.

I 16 characters x l line (When N=0, 5×8 dot Font): When 16 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below. (Special Application 16 characters* 1 line, 5*8 Font only)

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address(hex)	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47
Shift Left	01	02	03	04	05	06	07	08	41	42	43	44	45	46	47	48
Shift Right	4F	00	01	02	03	04	05	06	3F	40	41	42	43	44	45	46

Note:

<1>Display Position 1~8 DDRAM: 00H~4FH, the first address is 00H. Shift Right：00H → 4FH → 4EH → 4DH …… 3FH → 3EH → 3DH …… 01H → 00H → 4FH.

<2>Display Position 9~16 DDRAM: 00H~4FH, the first address is 40H. Shift Right: 40H → 3FH → 3EH → 3DH ……→ 00H → 4FH → 4EH →4DH …… 41H → 40H →3FH.

(d) 20 characters x 1 line (5×8 dot Font, 5×10 dot Font): When 20 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DDRAM Address(hex)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
Shift Right	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12

Case2: 2-Line Display (N=1，5×8 dot Font)

The Number of Characters displayed is less than 40 x 2 lines When the number of characters displayed is less than 40 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 40x8bits DDRAM space: 1st line is 00H to 27H; 2nd line is 40H to 67H. Please refer the figure below.

Display Position(Digit)	1	2	3	4	5	……	36	37	38	39	40
DDRAM Address(hex)	00	01	02	03	04	……	23	24	25	26	27
	40	41	42	43	44	……	63	64	65	66	67

(a) 8 characters x 2 lines: The relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8
DDRAM Address(hex)	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
Shift Left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
Shift Right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

(b) 12 characters x 2 lines: The relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12
DDRAM Address(hex)	00	01	02	03	04	05	06	07	08	09	0A	0B
	40	41	42	43	44	45	46	47	48	49	4A	4B
Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C
	41	42	43	44	45	46	47	48	49	4A	4B	4C
Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A
	67	40	41	42	43	44	45	46	47	48	49	4A

I16 characters x 2 lines: The relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address(hex)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(d) 20 characters x 2 lines: The relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position(Digit)	1	2	3	4	5	·····	16	17	18	19	20
DDRAM Address(hex)	00	01	02	03	04		0F	10	11	12	13
	40	41	42	43	44	·····	4F	50	51	52	53
Shift Left	01	02	03	04	05	·····	10	11	12	13	14
	41	42	43	44	45	·····	50	51	52	53	54
Shift Right	27	00	01	02	03	·····	0E	0F	10	11	12
	67	40	41	42	43	·····	4E	4F	40	51	52

(e) 20 characters x 1 line: When 20 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DDRAM Address(hex)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12

Case 3: 40-Character x 2 Lines Display (Cascade Mode, N=1, 5×8 dot Font)

SH1111 (Master) can be extended to display 40 characters x 2 lines by cascade the other SH1111 (Slave). When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position(Digit)	1	2	3	4	·····	17	18	19	20	21	22	23	24	·····	37	38	39	40
DDRAM Address(hex)	00	01	02	03	·····	10	11	12	13	14	15	16	17	·····	24	25	26	27
	40	41	42	43	·····	50	51	52	53	54	55	56	57	·····	64	65	66	67
	SH1111 display (Master)									Cascade Second SH1111 (Slave)								
Shift Left	01	02	03	04	·····	11	12	13	14	15	16	17	18	·····	25	26	27	00
	41	42	43	44	·····	51	52	53	54	55	56	57	58	·····	65	66	67	40
Shift Right	27	00	01	02	·····	0F	10	11	12	13	14	15	16	·····	23	24	25	26
	67	40	41	42	·····	4F	50	51	52	53	54	55	56	·····	63	64	65	66

Case 4: 20-Character x 2 Lines Display (N=0, 5×10 dot Font)

Display Position(Digit)	1	2	3	4	5	·····	16	17	18	19	20
DDRAM Address(hex)	00	01	02	03	04		0F	10	11	12	13
	14	15	16	17	18	·····	23	24	25	26	27
Shift Left	01	02	03	04	05	·····	10	11	12	13	14
	15	16	17	18	19	·····	24	25	26	27	28
Shift Right	4F	00	01	02	03	·····	0E	0F	10	11	12
	13	14	15	16	17	·····	22	23	24	25	26

Case 5: 16-Character x 4 Lines Display (N=1, 5×8 dot Font)

SH1111 can display 16 characters x 4 lines. When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position(Digit)	1	2	3	4	5	·····	12	13	14	15	16
DDRAM Address(hex)	00	01	02	03	04	·····	0B	0C	0D	0E	0F
	40	41	42	43	44	·····	4B	4C	4D	4E	4F
	10	11	12	13	14	·····	1B	1C	1D	1E	1F
	50	51	52	53	54	·····	5B	5C	5D	5E	5F
Shift Left	01	02	03	04	05	·····	0C	0D	0E	0F	10
	41	42	43	44	45	·····	4C	4D	4E	4F	50
	11	12	13	14	15	·····	1C	1D	1E	1F	20
	51	52	53	54	55	·····	5C	5D	5E	5F	60
Shift Right	27	00	01	02	03	·····	0A	0B	0C	0D	0E
	67	40	41	42	43	·····	4A	4B	4C	4D	4E
	0F	10	11	12	13	·····	1A	1B	1C	1D	1E
	4F	50	51	52	53	·····	5A	5B	5C	5D	5E

Case 6: 20-Character x 4 Lines Display (N=1, 5×8 dot Font)

SH1111 can display 20 characters x 4 lines. When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position(Digit)	1	2	3	4	5	·····	16	17	18	19	20
DDRAM Address(hex)	00	01	02	03	04	·····	0F	10	11	12	13
	40	41	42	43	44	·····	4F	50	51	52	53
	14	15	16	17	18	·····	23	24	25	26	27
	54	55	56	57	58	·····	63	64	65	66	67
Shift Left	01	02	03	04	05	·····	10	11	12	13	14
	41	42	43	44	45	·····	50	51	52	53	54
	15	16	17	18	19	·····	24	25	26	27	00
	55	56	57	58	59	·····	64	65	66	67	40
Shift Right	27	00	01	02	03	·····	0E	0F	10	11	12
	67	40	41	42	43	·····	4E	4F	50	51	52
	13	14	15	16	17	·····	22	23	24	25	26
	53	54	55	56	57	·····	62	63	64	65	66

Graphic Mode Addressing——Graphic Display Data RAM (GDDRAM)

SH1111 provides not only character mode but also graphic mode. User can fill in 100x32 data in embedded RAM to display graphic. Graphic mode addressing is different from character mode. Use DDRAM address instruction to set Page address of Graphic mode and CGRAM address instruction to set Column Address of Graphic mode.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Page Address	0	1	0	0	0	0	PAD1	PAD0
Column Address	1	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1	CAD0

Page Address	Data	1	2	3	4	……	……	97	98	99	100	Line Address	OLED OUTPUT CMS=0	OLED OUTPUT CMS=1
Page Address = 01000001	D0	Page Address = 01000000 Col Address = 10000000	Page Address = 01000000 Col Address = 10000001	Page Address = 01000000 Col Address = 10000010	Page Address = 01000000 Col Address = 10000011	……	……	Page Address = 01000000 Col Address = 11100000	Page Address = 01000000 Col Address = 11100001	Page Address = 01000000 Col Address = 11100010	Page Address = 01000000 Col Address = 11100011	00H	COM1	COM32
	D1											01H	COM2	COM31
	D2											02H	COM3	COM30
	D3											03H	COM4	COM29
	D4											04H	COM5	COM28
	D5											05H	COM6	COM27
	D6											06H	COM7	COM26
	D7											07H	COM8	COM25
Page Address = 01000001	D0	Page Address = 01000001 Col Address = 10000000	Page Address = 01000001 Col Address = 10000001	Page Address = 01000001 Col Address = 10000010	Page Address = 01000001 Col Address = 10000011	……	……	Page Address = 01000001 Col Address = 11100000	Page Address = 01000001 Col Address = 11100001	Page Address = 01000001 Col Address = 11100010	Page Address = 01000001 Col Address = 11100011	08H	COM9	COM24
	D1											09H	COM10	COM23
	D2											0AH	COM11	COM22
	D3											0BH	COM12	COM21
	D4											0CH	COM13	COM20
	D5											0DH	COM14	COM19
	D6											0EH	COM15	COM18
	D7											0FH	COM16	COM17
Page Address = 01000010	D0	Page Address = 01000010 Col Address = 10000000	Page Address = 01000010 Col Address = 10000001	Page Address = 01000010 Col Address = 10000010	Page Address = 01000010 Col Address = 10000011	……	……	Page Address = 01000010 Col Address = 11100000	Page Address = 01000010 Col Address = 11100001	Page Address = 01000010 Col Address = 11100010	Page Address = 01000010 Col Address = 11100011	10H	COM17	COM16
	D1											11H	COM18	COM15
	D2											12H	COM19	COM14
	D3											13H	COM20	COM13
	D4											14H	COM21	COM12
	D5											15H	COM22	COM11
	D6											16H	COM23	COM10
	D7											17H	COM24	COM9
Page Address = 01000011	D0	Page Address = 01000011 Col Address = 10000000	Page Address = 01000011 Col Address = 10000001	Page Address = 01000011 Col Address = 10000010	Page Address = 01000011 Col Address = 10000011	……	……	Page Address = 01000011 Col Address = 11100000	Page Address = 01000011 Col Address = 11100001	Page Address = 01000011 Col Address = 11100010	Page Address = 01000011 Col Address = 11100011	18H	COM25	COM8
	D1											19H	COM26	COM7
	D2											1AH	COM27	COM6
	D3											1BH	COM28	COM5
	D4											1CH	COM29	COM4
	D5											1DH	COM30	COM3
	D6											1EH	COM31	COM2
	D7											1FH	COM32	COM1

OLED OUTPUT	SEG1	SEG2	SEG3	SEG4	……	……	SEG97	SEG98	SEG99	SEG100	SHL=0	
OLED OUTPUT	SEG100	SEG99	SEG98	SEG96	……	……	SEG4	SEG3	SEG2	SEG1	SHL=1	

Figure.11

The Graphic Mode Page Address Circuit

As shown in Figure.11, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Graphic Mode Column Address Circuit

As shown in Figure.11, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 43H to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table.7, the Column re-mapping (SHL) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table.7

Segment Output	SEG1		SEG100
SHL = "0"	0 (H) →	Column Address	→63 (H)
SHL = "1"	63 (H) ←	Column Address	← 0 (H)

The Graphic Mode Line Address Circuit

The line address circuit, as shown in Figure.12, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM32 output for SH1111, when the common output mode is reversed. The display area is a 32-line area for the SH1111 from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 0EH).

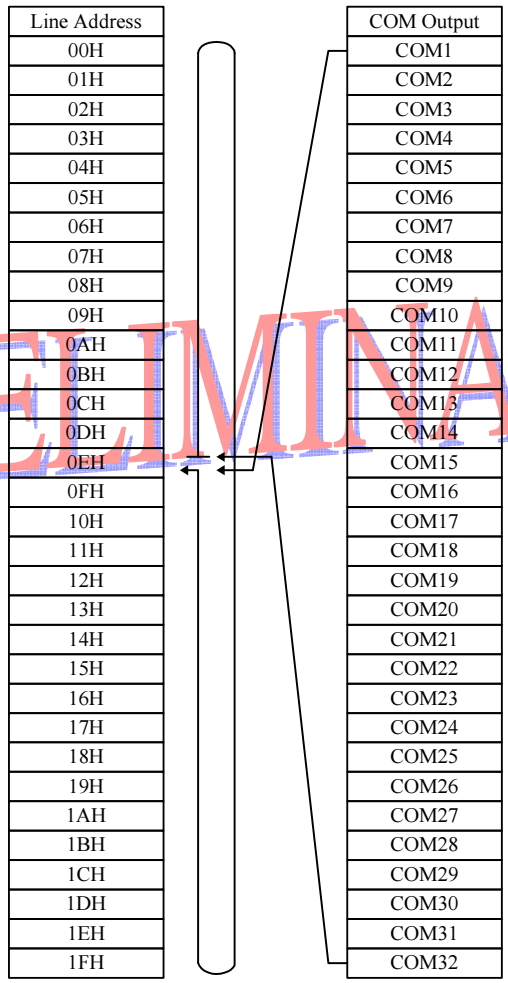
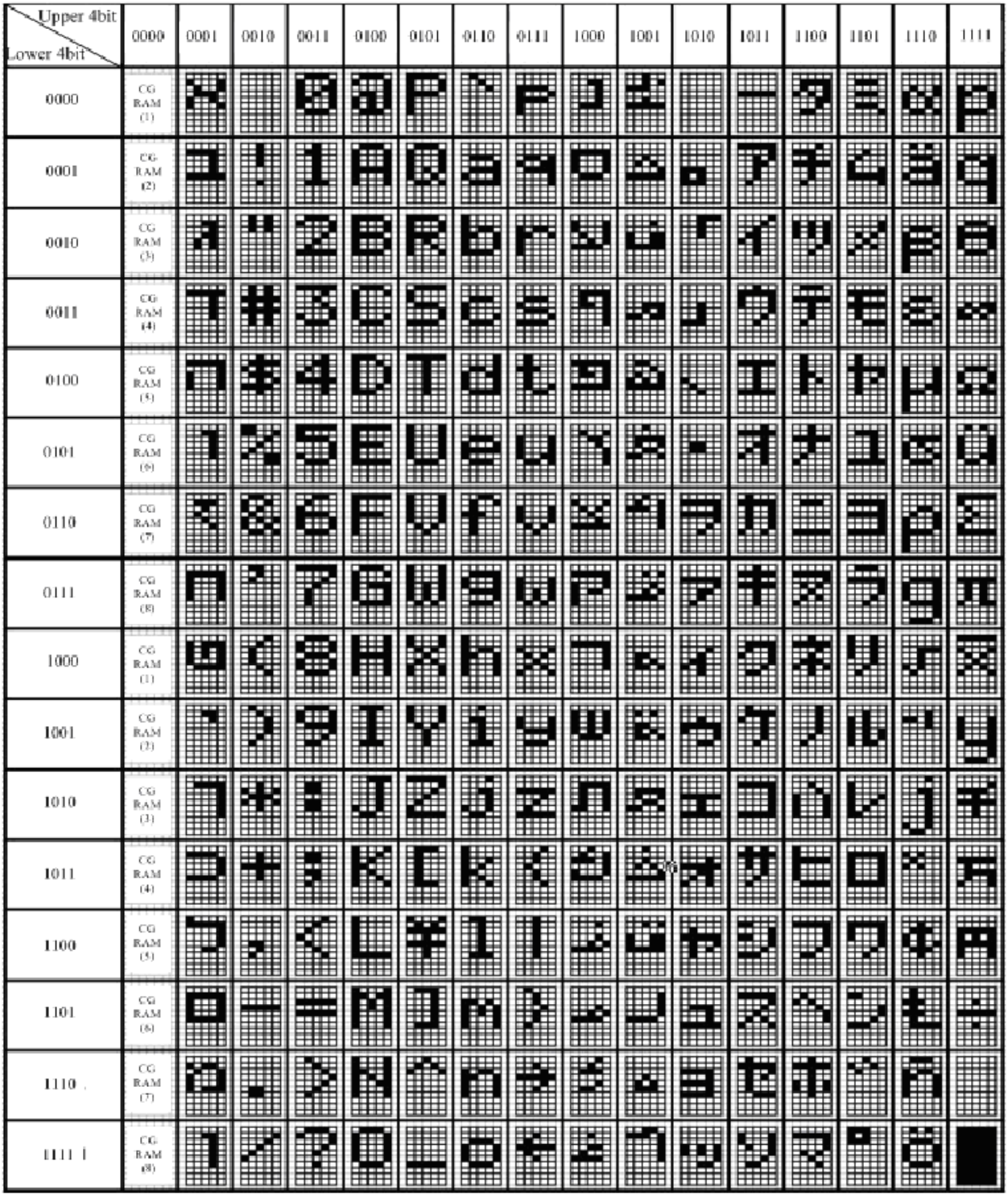


Figure.12 Display Start Line Setting Function

Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) is used to generate either 5 x 8 dots or 5 x 10 dots character patterns from 8-bit character codes. SH1111 build in four set of font tables as “Western European-I”, ”English Japanese”, “English Russian” and “Western European-II” . Character font can be selected by programming FT[2:0].

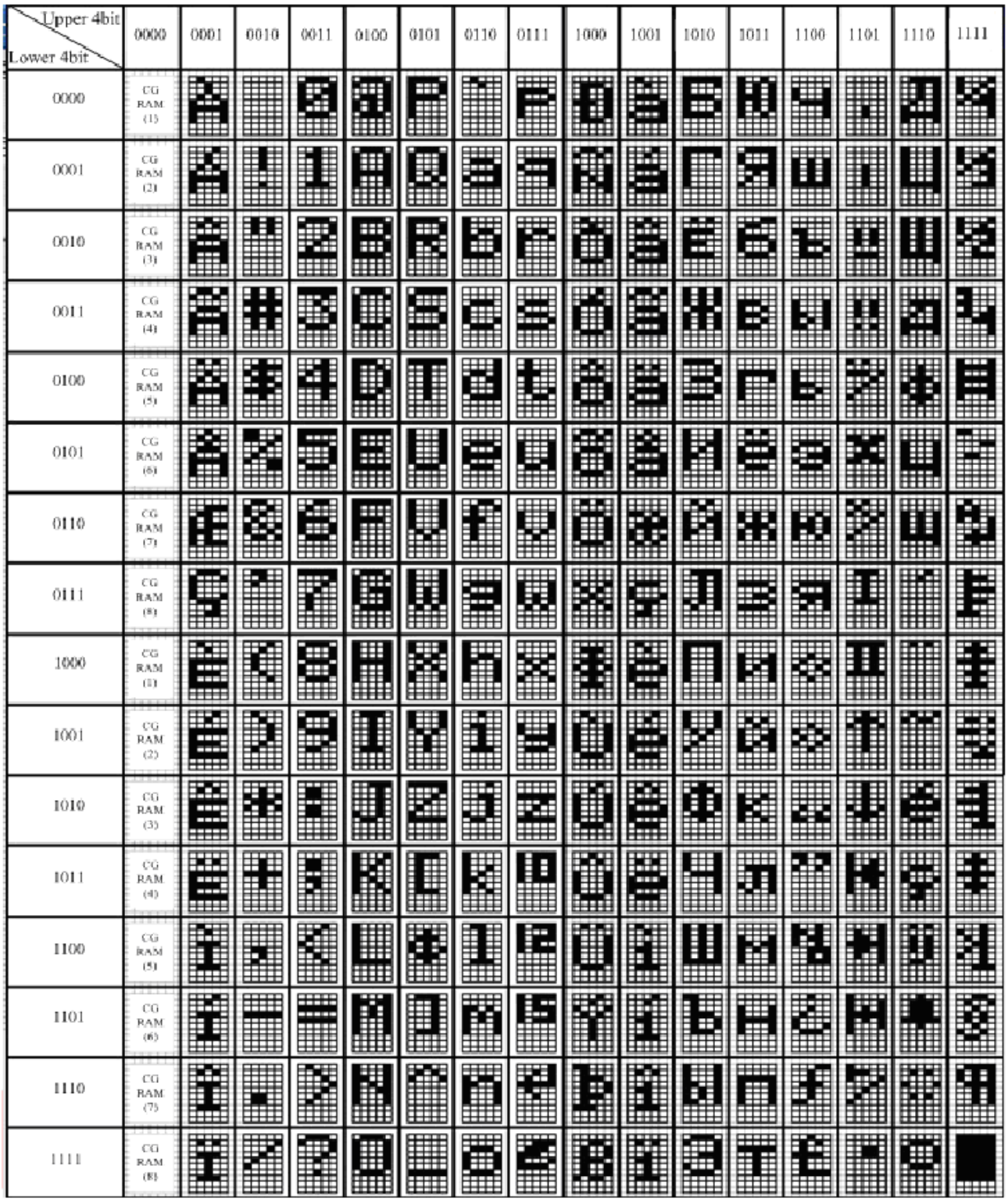
ENGLISH_JAPANESE CHARACTER FONT TABLE (default FT[1:0]= 00).



WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	CG RAM (2)															
0010	CG RAM (3)															
0011	CG RAM (4)															
0100	CG RAM (5)															
0101	CG RAM (6)															
0110	CG RAM (7)															
0111	CG RAM (8)															
1000	CG RAM (1)															
1001	CG RAM (2)															
1010	CG RAM (3)															
1011	CG RAM (4)															
1100	CG RAM (5)															
1101	CG RAM (6)															
1110	CG RAM (7)															
1111	CG RAM (8)															

ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)



WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=11)

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	CG RAM (2)															
0010	CG RAM (3)															
0011	CG RAM (4)															
0100	CG RAM (5)															
0101	CG RAM (6)															
0110	CG RAM (7)															
0111	CG RAM (8)															
1000	CG RAM (1)															
1001	CG RAM (2)															
1010	CG RAM (3)															
1011	CG RAM (4)															
1100	CG RAM (5)															
1101	CG RAM (6)															
1110	CG RAM (7)															
1111	CG RAM (8)															

Character Generator RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate either 5 x 8 dot or 5 x 10 dot character patterns. It can generate eight 5 x 8 dot character patterns or four 5 x 10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 8 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	1	1	1	1	0	Character Pattern 1
												0	0	1		*	*	*	1				1	
												0	1	0		*	*	*	1				1	
												0	1	1		*	*	*	1	1	1	1		
												1	0	0		*	*	*	1		1			
												1	0	1		*	*	*	1			1		
												1	1	0		*	*	*	1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	0	0	0	1	Character Pattern 2
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	1	1	1	1	1	
												0	1	1		*	*	*	0	0	1	0	0	
												1	0	0		*	*	*	1	1	1	1	1	
												1	0	1		*	*	*	0	0	1	0	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	•	•	•		•	•	•	•	•	•		*	*	*	•	•	•	•	•	Character Pattern 3~7
					•	•	•		•	•	•	•	•	•					•	•	•	•	•	
					•	•	•		•	•	•	•	•	•					•	•	•	•	•	
					•	•	•		•	•	•	•	•	•					•	•	•	•	•	
0	0	0	0	*	1	1	1		1	1	1	0	0	0		*	*	*	0	1	1	1	1	Character Pattern 8
												0	0	1		*	*	*	1	0	0	0	0	
												0	1	0		*	*	*	1	0	0	0	0	
												0	1	1		*	*	*	0	1	1	1	0	
												1	0	0		*	*	*	0	0	0	0	1	
												1	0	1		*	*	*	0	0	0	0	1	
												1	1	0		*	*	*	1	1	1	1	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position

Notes:
1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits – 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3 bits: 8 types)
4. If the CGRAM Data is set to “1”, then the selection is displayed. If the CGRAM is set to “0”, there no selection is made.
5. The CGRAM Address Bits 0 to 2 are used to define the character pattern line position. The 8th line is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to “0”. If any of the 8th line CGRAM data bits 0 to 4 is set to “1”, the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 is set to “0”, then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this, the first Character Pattern shown above I can be displayed when the Character Code is 00H or 08H.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 10 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0	
High						Low			High				Low		High						Low		
0	0	0	0	*	0	0	*		0	0	0	0	0	0	*	*	*	0	0	1	0	0	Character Pattern 1
											0	0	0	1	*	*	*	0	1	1	1	0	
											0	0	1	0	*	*	*	1	0	1	0	1	
											0	0	1	1	*	*	*	1	0	1	0	0	
											0	1	0	0	*	*	*	0	1	1	0	0	
											0	1	0	1	*	*	*	0	0	1	1	0	
											0	1	1	0	*	*	*	0	0	1	0	1	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	
0	0	0	0	*	•	•	*		•	•	•	•	•	•	*	*	*	•	•	•	•	•	Character Pattern 2~3
					•	•			•	•	•	•	•	•	*	*	*	•	•	•	•	•	
					•	•			•	•	•	•	•	•	*	*	*	•	•	•	•	•	
0	0	0	0	*	1	1	*		1	1	0	0	0	0	*	*	*	1	0	1	0	1	Character Pattern 4
											0	0	0	1	*	*	*	1	1	1	1	1	
											0	0	1	0	*	*	*	1	1	1	1	1	
											0	0	1	1	*	*	*	1	1	1	1	1	
											0	1	0	0	*	*	*	0	1	1	1	0	
											0	1	0	1	*	*	*	0	0	1	0	0	
											0	1	1	0	*	*	*	0	0	1	0	0	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	

Notes:
1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits – 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 1 and 2 correspond to the CGRAM Address Bits – 4 and 5 respectively (2 bits: 4 types)
4. If the CGRAM Data is set to “1”, then the selection is displayed. If the CGRAM is set to “0”, there no selection is made.
5. The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to “0”. If any of the 11th line CGRAM data bits 0 to 4 is set to “1”, the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to “0”, then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit – 0 and 3 are not relevant and will not have any effect on the character display. Because of this, the Character Pattern shown above ($) can be displayed when the Character Code is 00H, 01H, 08H or 09H.

Common and Segment Drivers

SH1111 provides 32 Common Drivers and 100 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the waveform automatically. A non-selection waveform will be outputted by the rest of the Common outputs.

Cursor/Blink Control Circuit

The cursor or character blinking is generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM (DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address Counter	0	0	0	0	1	1	1

Case 1: For 1-line Display

Example: When the Address Counter (AC) is set to 0EH, the cursor position is displayed at DDRAM Address 0EH.

Display Position	1	2	3	4	5	·····	14	15	16	·····	37	38	39	40
DDRAM Address (Hexadecimal)	00H	01H	02H	03H	04H	·····	0DH	**0EH**	0FH	·····	25H	26H	27H	28H

Cursor Position

Note:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

Case 2: For 2-line Display

Example: When the Address Counter (AC) is set to 46H, the cursor position is displayed at DDRAM Address 46H.

Display Position	1	2	3	4	5	6	7	8	9	·····	17	18	19	20
DDRAM Address (Hexadecimal)	00H	01H	02H	03H	04H	06H	07H	08H	09H	·····	10H	11H	12H	13H
	40	41	42	43	44	45	**46H**	47H	48H	·····	50H	51H	52H	53H

Cursor Position

Note:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

Interface to OLED

(1) Character Font and Number of Lines.
The SH1111 provides a 5X8 dot character font 1-line mode, a 5X10 dot character font 1-line mode, a 5X8 dot character font 2-line mode, a 5X10 dot character font 2-line mode, a 5X8 dot character font 4-line mode as shown in the table below.
Five types of common signals are available as displayed in the table. The number of lines and the font type can be selected by the program and pad option.

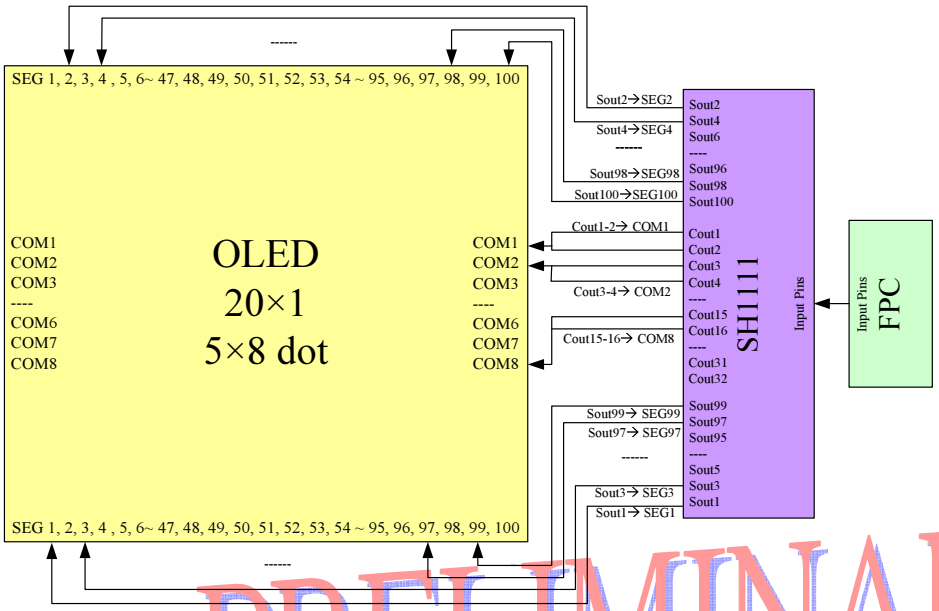
Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5×7 dots + Cursor (or 5×8 dots)	8	1/8
1	5×10 dots + Cursor	11	1/11
2	5×7 dots + Cursor (or 5×8 dots)	16	1/16
2	5×10 dots + Cursor	22	1/22
4	5×7 dots + Cursor (or 5×8 dots)	32	1/32

(2) Connection to OLED
The following 9 OLED connection examples show the various combinations between characters and lines. The various combinations can be select by pad option “GC”, “CAS_EN”, “CAS_MS”, “CHAR16”, “RESOL” and register option “N”, “F” (Function Set Command).
The various combinations between SH1111 and OLED Panel are displayed in the following table.

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
1	20 character×1 line, 5×8 dot	0	0	*	0	0	0	0	Single Chip Application, No Slave						
2	20 character×2 line, 5×8 dot	0	0	*	0	0	1	-	Single Chip Application, No Slave						
3	20 character×4 line, 5×8 dot	0	0	*	0	1	1	-	Single Chip Application, No Slave						
4	40 character×1 line, 5×8 dot	0	1	1	0	0	0	0	0	1	0	0	0	0	0
5	40 character×2 line, 5×8 dot	0	1	1	0	0	1	-	0	1	0	0	0	1	-
6	20 character×1 line,5×10 dot	0	0	*	0	0	0	1	Single Chip Application, No Slave						
7	20 character×2 line,5×10 dot	0	0	*	0	1	0	1	Single Chip Application, No Slave						
8	40 character×1 line,5×10 dot	0	1	1	0	0	0	1	0	1	0	0	0	0	1
9	16 character ×1 line,5×8 dot	0	0	*	1	0	-	-	Single Chip Application, No Slave						
10	16 character ×4 line,5×8 dot	0	0	*	1	1	1	-	Single Chip Application, No Slave						
11	100×32 dot matrix (Graphic Mode)	1	0	*	*	*	-	-	Single Chip Application, No Slave						

Note:
1. The display resolution of Graphic Mode can select by register “Graphic Duty [3:0]”.
2. * = Connect to GND or VDD1. User can not floating those pins.
3. - = Set this bit to “0” or “1”. When N = 1(2-line display mode), no mater F = 0 or 1, the 5 x 8 dot character font is selected.
4. Single chip application, CK_SFT, CK_LA, MS_D and MS_FM must be floating.
5. When use cascade mode, the COM1~32 of master and COM1~32 of slave can not be connect together.

Case1: 20 characters X 1 line, 5 X 8 Font (1/8 duty, single chip mode)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



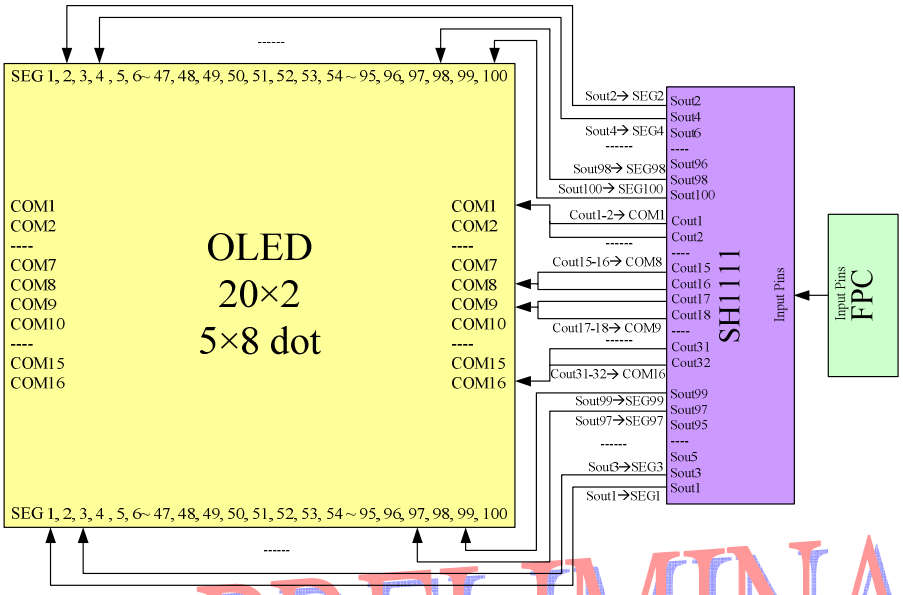
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1,Cout2	COM1
	Cout3,Cout4	COM2
	Cout5,Cout6	COM3
	Cout7,Cout8	COM4
	Cout9,Cout10	COM5
	Cout11,Cout12	COM6
	Cout13,Cout14	COM7
	Cout15,Cout16	COM8
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
1	20 character×1 line, 5×8 dot	0	0	*	0	0	0	0	Single Chip Application, No Slave						

Case2: 20 characters X 2 line, 5 X 8 Font (1/16 duty, single chip mode)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



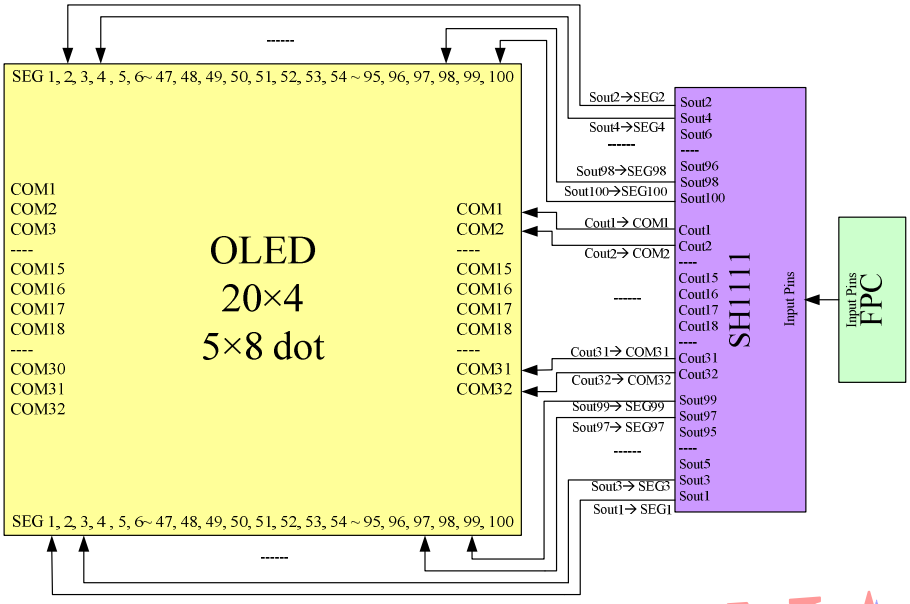
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1,Cout2	COM1
	Cout3,Cout4	COM2
	Cout5,Cout6	COM3
	Cout7,Cout8	COM4
	……	……
	Cout25,Cout26	COM13
	Cout27,Cout28	COM14
	Cout29,Cout30	COM15
	Cout31,Cout32	COM16
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
2	20 character×2 line, 5×8 dot	0	0	*	0	0	1	-	Single Chip Application, No Slave						

Case3: 20 characters X 4 line, 5 X 8 Font (1/32 duty, single chip mode)



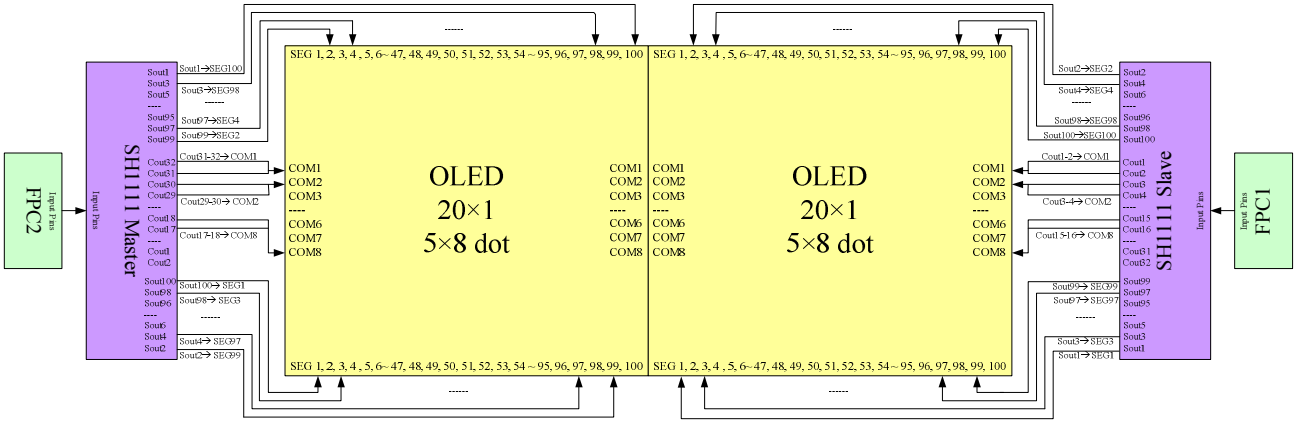
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table: (Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1	COM1
	Cout2	COM2
	Cout3	COM3
	Cout4	COM4
	……	……
	Cout29	COM29
	Cout30	COM30
	Cout31	COM31
	Cout32	COM32
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
3	20 character×4 line, 5×8 dot	0	0	*	0	1	1	-	Single Chip Application, No Slave						

Case4: 40 characters X 1 line, 5 X 8 Font (1/8 duty, cascade mode application)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

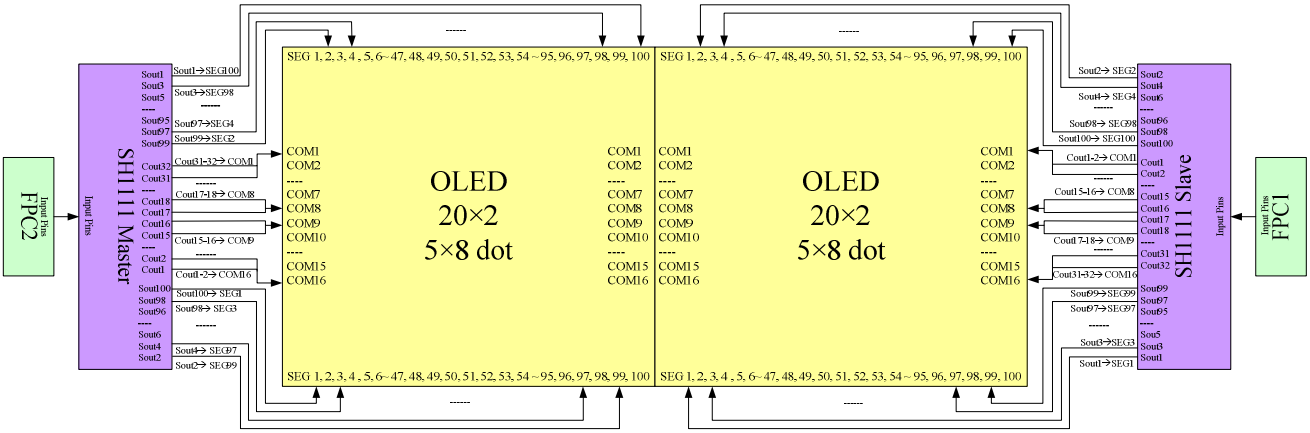
	Master & OLED Panel		Slave & OLED Panel	
	Master Output	OLED Panel Input	Slave Output	OLED Panel Input
Relationship of COM	Cout17,Cout18	COM8	Cout1,Cout2	COM1
	Cout19,Cout20	COM7	Cout3,Cout4	COM2
	Cout21,Cout22	COM6	Cout5,Cout6	COM3
	Cout23,Cout24	COM5	Cout7,Cout8	COM4
	Cout25,Cout26	COM4	Cout9,Cout10	COM5
	Cout27,Cout28	COM3	Cout11,Cout12	COM6
	Cout29,Cout30	COM2	Cout13,Cout14	COM7
	Cout31,Cout32	COM1	Cout15,Cout16	COM8
Relationship of SEG (Odd Number)	Sout1	SEG100	Sout1	SEG1
	Sout3	SEG98	Sout3	SEG3
	Sout5	SEG96	Sout5	SEG5
	……	……	……	……
	Sout95	SEG6	Sout95	SEG95
	Sout97	SEG4	Sout97	SEG97
	Sout99	SEG2	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG99	Sout2	SEG2
	Sout4	SEG97	Sout4	SEG4
	Sout6	SEG95	Sout6	SEG6
	……		……	……
	Sout96	SEG5	Sout96	SEG96
	Sout98	SEG3	Sout98	SEG98
	Sout100	SEG1	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
4	40 character×1 line, 5×8 dot	0	1	1	0	0	0	0	0	1	0	0	0	0	0

Note:
When use this mode, the COM1~32 of master and COM1~32 of slave can not be connect together.

Case5: 40 characters X 2 line, 5 X 8 Font (1/16 duty, cascade mode application)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

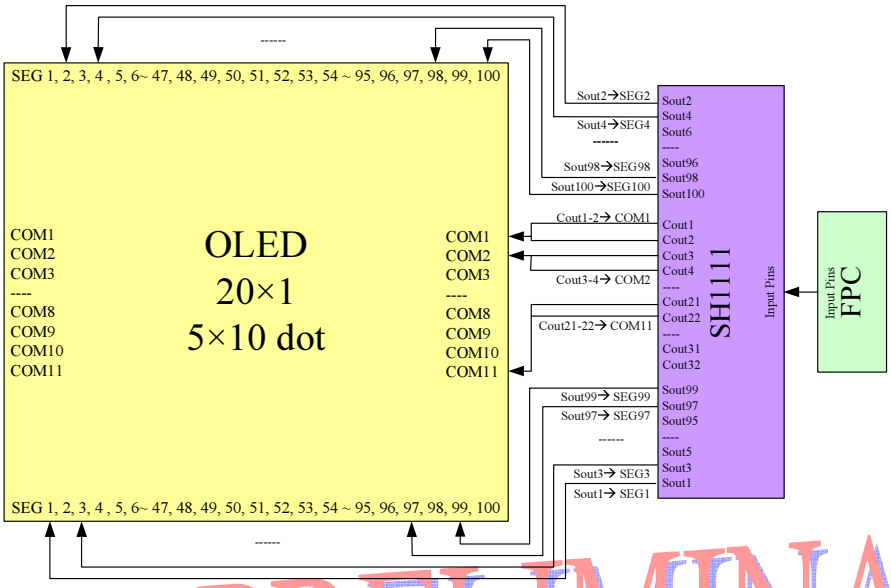
	Master & OLED Panel		Slave & OLED Panel	
	Master Output	OLED Panel Input	Slave Output	OLED Panel Input
Relationship of COM	Cout1,Cout2	COM16	Cout1,Cout2	COM1
	Cout3,Cout4	COM15	Cout3,Cout4	COM2
	Cout5,Cout6	COM14	Cout5,Cout6	COM3
	Cout7,Cout8	COM13	Cout7,Cout8	COM4
	Cout9,Cout10	COM12	Cout9,Cout10	COM5
	Cout11,Cout12	COM11	Cout11,Cout12	COM6
	Cout13,Cout14	COM10	Cout13,Cout14	COM7
	Cout15,Cout16	COM9	Cout15,Cout16	COM8
	Cout17,Cout18	COM8	Cout17,Cout18	COM9
	Cout19,Cout20	COM7	Cout19,Cout20	COM10
	Cout21,Cout22	COM6	Cout21,Cout22	COM11
	Cout23,Cout24	COM5	Cout23,Cout24	COM12
	Cout25,Cout26	COM4	Cout25,Cout26	COM13
	Cout27,Cout28	COM3	Cout27,Cout28	COM14
	Cout29,Cout30	COM2	Cout29,Cout30	COM15
	Cout31,Cout32	COM1	Cout31,Cout32	COM16
Relationship of SEG (Odd Number)	Sout1	SEG100	Sout1	SEG1
	Sout3	SEG98	Sout3	SEG3
	Sout5	SEG96	Sout5	SEG5
	……	……	……	……
	Sout95	SEG6	Sout95	SEG95
	Sout97	SEG4	Sout97	SEG97
	Sout99	SEG2	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG99	Sout2	SEG2
	Sout4	SEG97	Sout4	SEG4
	Sout6	SEG95	Sout6	SEG6
	……		……	……
	Sout96	SEG5	Sout96	SEG96
	Sout98	SEG3	Sout98	SEG98
	Sout100	SEG1	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
5	40 character×2 line, 5×8 dot	0	1	1	0	0	1	-	0	1	0	0	0	1	-

Note:
When use this mode, the COM1~32 of master and COM1~32 of slave can not be connect together.

Case6: 20 characters X 1 line, 5 X 10 Font (1/11 duty)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



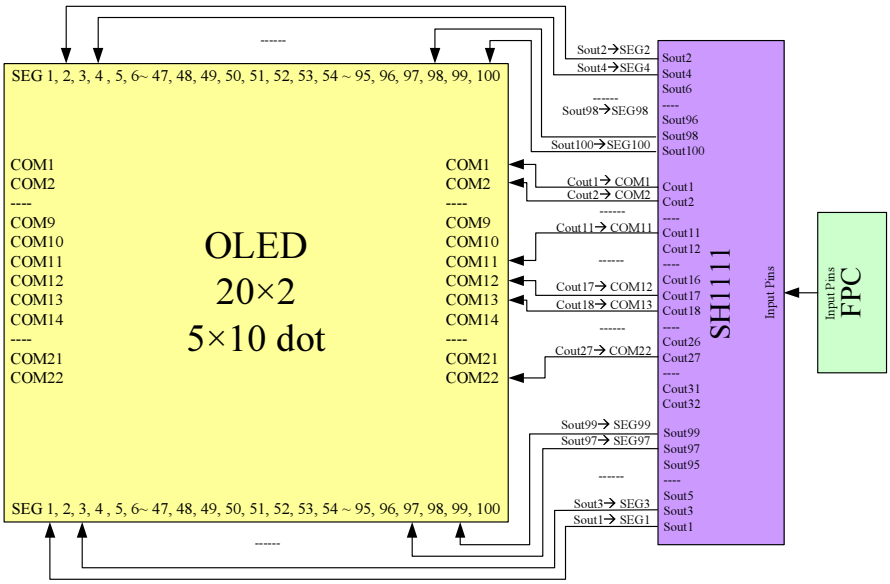
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1,Cout2	COM1
	Cout3,Cout4	COM2
	Cout5,Cout6	COM3
	Cout7,Cout8	COM4
	Cout9,Cout10	COM5
	Cout11,Cout12	COM6
	Cout13,Cout14	COM7
	Cout15,Cout16	COM8
	Cout17,Cout18	COM9
	Cout19,Cout20	COM10
	Cout21,Cout22	COM11
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	.....	.....
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	.....	.....
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
6	20 character×1 line,5×10 dot	0	0	*	0	0	0	1	Single Chip Application, No Slave						

Case7: 20 characters X 2 line, 5 X 10 Font (1/22 duty)



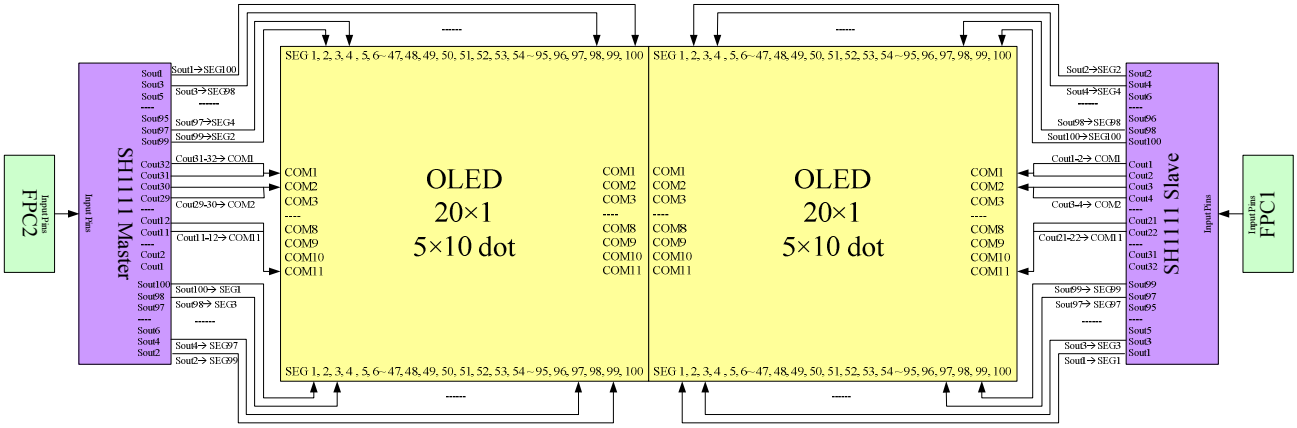
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1	COM1
	Cout2	COM2
	Cout3	COM3
	.....	.....
	Cout9	COM9
	Cout10	COM10
	Cout11	COM11
	COM17	COM12
	COM18	COM13
	COM19	COM14
	.....	.....
	COM25	COM20
	COM26	COM21
	COM27	COM22
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	.....	.....
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	.....	.....
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
7	20 character×2 line,5×10 dot	0	0	*	0	1	0	1	Single Chip Application, No Slave						

Case8: 40 characters X 1 line, 5 X 10 Font (1/11 duty, Cascade application)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

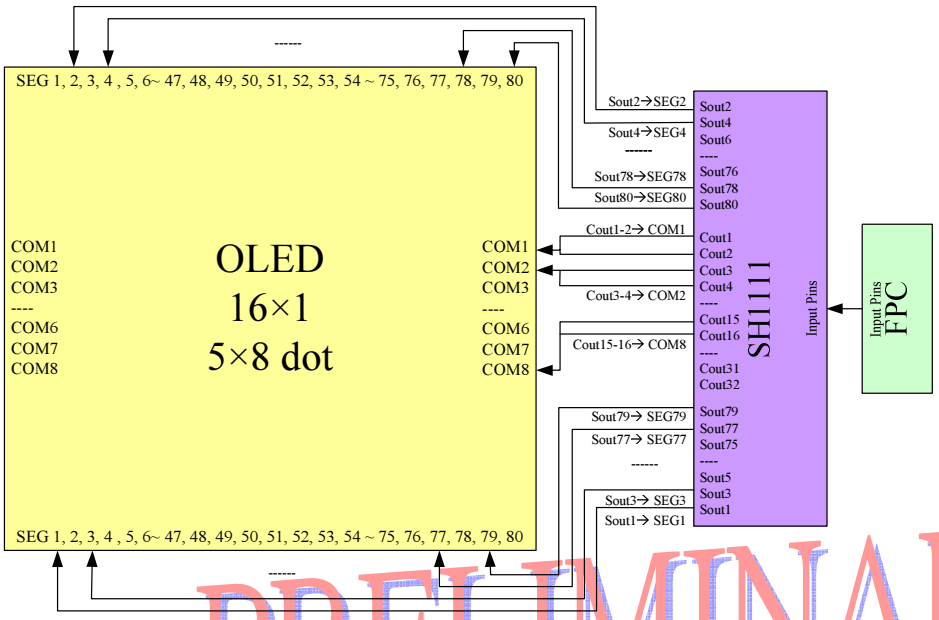
	Master & OLED Panel		Slave & OLED Panel	
	Master Output	OLED Panel Input	Slave Output	OLED Panel Input
Relationship of COM	Cout11,Cout12	COM11	Cout1,Cout2	COM1
	Cout13,Cout14	COM10	Cout3,Cout4	COM2
	Cout15,Cout16	COM9	Cout5,Cout6	COM3
	Cout17,Cout18	COM8	Cout7,Cout8	COM4
	Cout19,Cout20	COM7	Cout9,Cout10	COM5
	Cout21,Cout22	COM6	Cout11,Cout12	COM6
	Cout23,Cout24	COM5	Cout13,Cout14	COM7
	Cout25,Cout26	COM4	Cout15,Cout16	COM8
	Cout27,Cout28	COM3	Cout17,Cout18	COM9
	Cout29,Cout30	COM2	Cout19,Cout20	COM10
	Cout31,Cout32	COM1	Cout21,Cout22	COM11
Relationship of SEG (Odd Number)	Sout1	SEG100	Sout1	SEG1
	Sout3	SEG98	Sout3	SEG3
	Sout5	SEG96	Sout5	SEG5
	……	……	……	……
	Sout95	SEG6	Sout95	SEG95
	Sout97	SEG4	Sout97	SEG97
	Sout99	SEG2	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG99	Sout2	SEG2
	Sout4	SEG97	Sout4	SEG4
	Sout6	SEG95	Sout6	SEG6
	……		……	……
	Sout96	SEG5	Sout96	SEG96
	Sout98	SEG3	Sout98	SEG98
	Sout100	SEG1	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
8	40 character×1 line,5×10 dot	0	1	1	0	0	0	1	0	1	0	0	0	0	1

Note:
When use this mode, the COM1~32 of master and COM1~32 of slave can not be connect together.

Case9: 16 characters X 1 line, 5 X 8 Font (1/8 duty, single chip mode)
In this mode, COM1~2 switch together, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~18, COM19~20, COM21～22，COM23～24, COM25~26, COM27~28, COM29~30 and COM31~32 switch together.



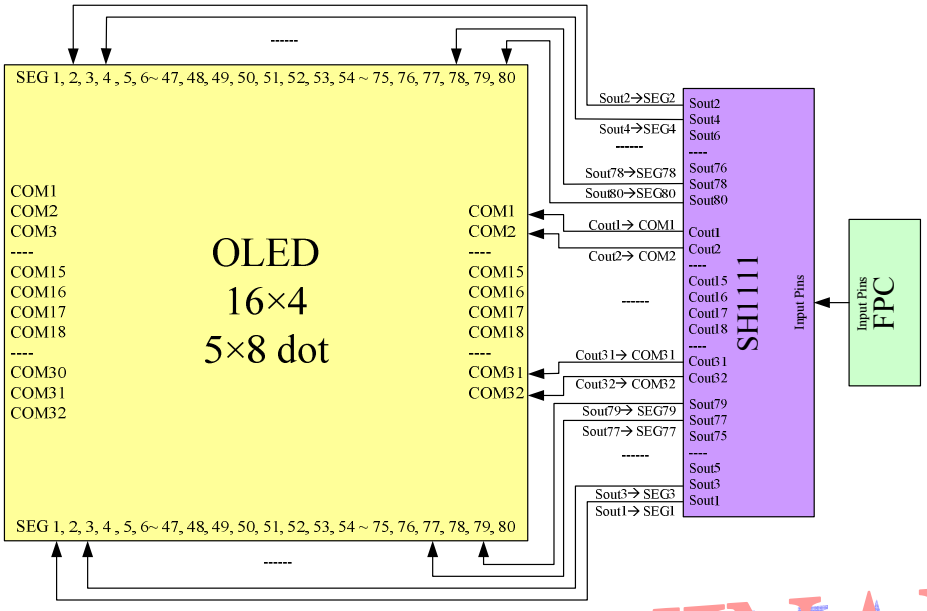
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32, Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1,Cout2	COM1
	Cout3,Cout4	COM2
	Cout5,Cout6	COM3
	Cout7,Cout8	COM4
	Cout9,Cout10	COM5
	Cout11,Cout12	COM6
	Cout13,Cout14	COM7
	Cout15,Cout16	COM8
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout75	SEG75
	Sout77	SEG77
	Sout79	SEG79
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout76	SEG76
	Sout78	SEG78
	Sout80	SEG80

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
9	16 character ×1 line,5×8 dot	0	0	*	1	0	-	-	Single Chip Application, No Slave						

Case10: 16 characters X 4 line, 5 X 8 Font (1/32 duty, single chip mode)



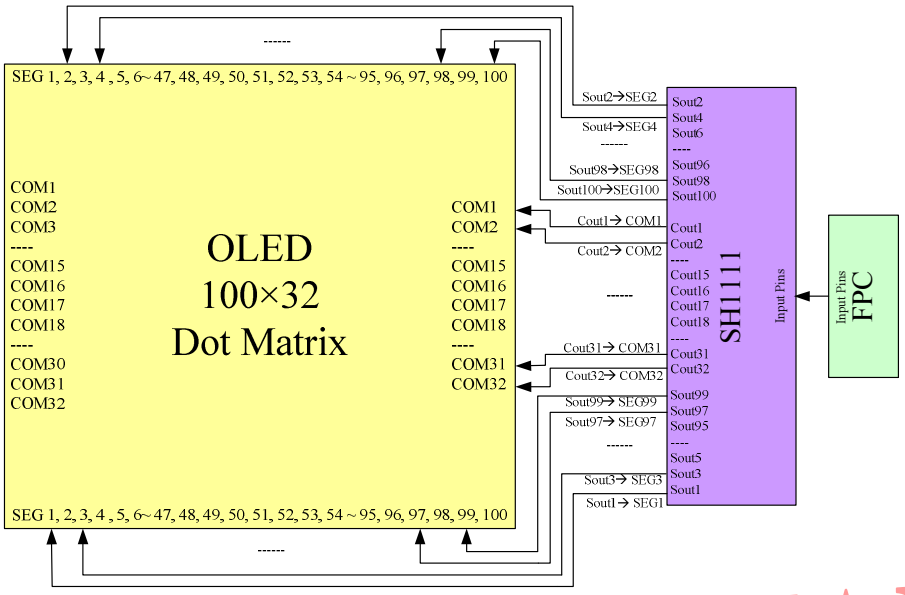
The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1	COM1
	Cout2	COM2
	Cout3	COM3
	Cout4	COM4
	……	……
	Cout29	COM29
	Cout30	COM30
	Cout31	COM31
	Cout32	COM32
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout75	SEG75
	Sout77	SEG77
	Sout79	SEG79
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout76	SEG76
	Sout78	SEG78
	Sout80	SEG80

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
10	16 character ×4 line,5×8 dot	0	0	*	1	1	1	-	Single Chip Application, No Slave						

Case11: 100×32 dot matrix(1/32 duty, single chip mode，GC=1)



The relationship between Master/Slave output COM&SEG and OLED Panel input COM&SEG show in the following table:
(Master/Slave output COM1~32 named Cout1~32. Master/Slave output SEG1~100 named Sout1~100.)

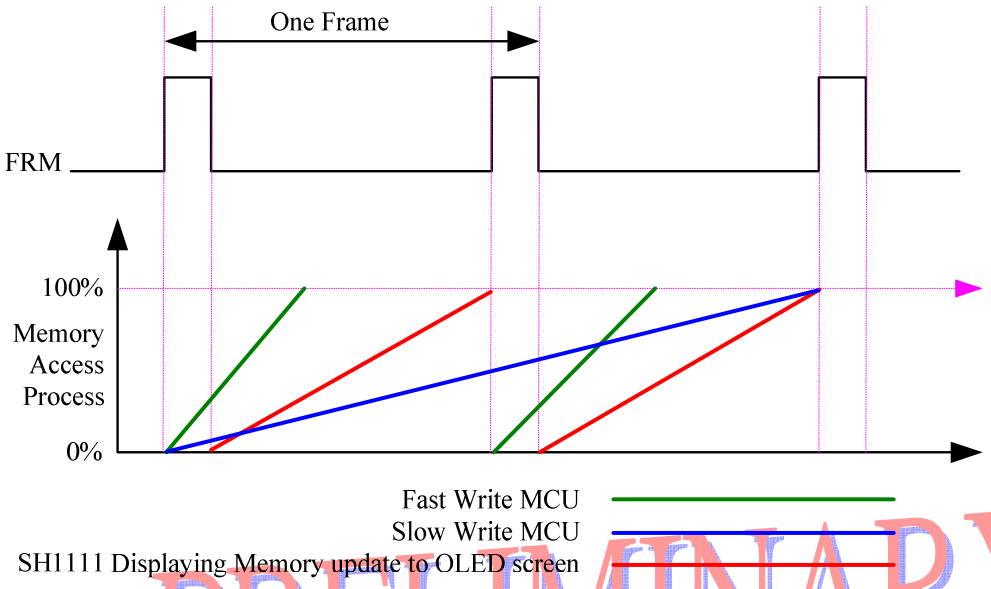
	Master & OLED Panel	
	Master Output	OLED Panel Input
Relationship of COM	Cout1	COM1
	Cout2	COM2
	Cout3	COM3
	Cout4	COM4
	……	……
	Cout29	COM29
	Cout30	COM30
	Cout31	COM31
	Cout32	COM32
Relationship of SEG (Odd Number)	Sout1	SEG1
	Sout3	SEG3
	Sout5	SEG5
	……	……
	Sout95	SEG95
	Sout97	SEG97
	Sout99	SEG99
Relationship of SEG (Even Number)	Sout2	SEG2
	Sout4	SEG4
	Sout6	SEG6
	……	……
	Sout96	SEG96
	Sout98	SEG98
	Sout100	SEG100

Pad Option and Register Option value are shown below:

Case	Resolution	Master							Slave						
		GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F	GC	CAS _EN	CAS _MS	CHAR16	RESOL	N	F
11	100×32 dot matrix (Graphic Mode)	1	0	*	*	*	-	-	Single Chip Application, No Slave						

FRM Synchronization

FRM synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FRM pulse and should be finished well before the rising edge of the next FRM pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FRM pulse and must be finished before the rising edge of the 3rd FRM pulse.

The Oscillator Circuit

This is a RC type oscillator (Figure. 13) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

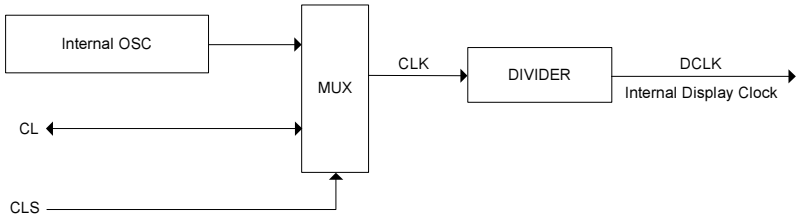


Figure. 13

DC- DC Voltage Converter / Charge Pump Regulator

This block accompanying only 2 external capacitors, is used to generate a 6.4V~12.0V voltage for OLED panel. This regulator can be turned ON/OFF by Pad Option VPPS.

VPPS PAD VALUE	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

Reset Circuit

When power is turned ON, SH1111 is initialized automatically by an internal reset circuit. The following items are set (default) during the initialization. The busy flag(BF) is kept in the busy state until the initialization. The busy state lasts for 10ms after VDD1 rises to 4.5V。

1. Display clear.
2. Function set:
   DL = 1: 8-bit interface data.
   N = 0: 1-line display.
   F = 0: 5*8 dot character font.
3. Display ON/OFF control:
   D = 0: Display off.
   C = 0: Cursor off.
   B = 0: Blinking off
4. Entry mode set:
   I/D = 1: Increase by 1.
   S = 0: No shift.
5. All register in Command Table2 are set to POR Value. Command Table2 POR Value is shown below.

Function	Control bit	Remarks
Divide Ratio/Oscillator Frequency Data Set	Oscillator Frequency = 0101 Divide Ratio = 0001	
Dis-charge /Pre-charge Period Mode Set	PDCVS=0: Dis-charge Period = 0010 Pre-charge Period = 0010 PDCVS=1: Dis-charge Period = 1111 Pre-charge Period = 1111	 2 DCLKs 2 DCLKs 15 DCLKs 15 DCLKs
VCOM Deselect Level Data Set	PDCVS = 0: VCOM = 35H PDCVS = 1: VCOM = 40H	
Contrast Control Set	PDCVS = 0: Contrast = 80H PDCVS = 1: Contrast = FFH	
Graphic Vertical scrolling set	Vertical scrolling = 0000	Start Line: COM1
Graphic duty set	Graphic duty = 1001	Normal Display
VPP Voltage Set	VPP[1:0] = 11	VPP = 12.0V
SEG Direction Set	SHL = 0	SEG1→SEG100
COM Direction Set	CMS = 0	COM1→COM32
Pump Times Set	DCS = 0	Pump 3 times
Software Set Font Table Enable	FTE = 0	Software set font table disable
Software Font Table Select	FTS[1:0] = 00	Font Table 1
Blinking Duty Set	BD[2:0] = 010	300ms

Commands

The SH1111 uses a combination of RS, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the $R/\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8 bit 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Clear Display: (01h)

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode (I/D="1"). S of entry mode does not change.

RS	$\overline{WR}$ ($R/\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1

2. Return Home: (02H – 03H)

It sets Display Data RAM Address "00H" in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

RS	$\overline{WR}$ ($R/\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	*

*: Do not care (0 or 1)

3. Entry Mode Set: (04H – 07H)

During writing and reading data, it defines cursor moving direction and shifts the display.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	I/D	S

I/D: The Increment / Decrement of DDRAM address (cursor or blink).

When I/D = "1", the DDRAM Address is incremented by "1" when a character code is written into or read from the DDRAM. An increment of 1 will move the cursor or blinking one step to the right. (POR)

When I/D = "0", the DDRAM is decremented by 1 when a character code is written into or read from the DDRAM. A decrement of 1 will move the cursor or blinking one step to the left.

Note: CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift Enter Display Control bit

This bit is used to shift the entire display.

When S = "1" and DDRAM write operation, the entire display is shifted to the right (when I/D = "0") or left (when I/D = "1").

When S = "0" or DDRAM read (CGRAM read/write) operation, the display is not shifted. (POR)

Ex1: I/D = "1", S = "1", Shift the display to the left.

		1	2	3	4	_	Initial display
	1	2	3	4	A	_	Input new character "A"
1	2	3	4	A	B	_	Input new character "B"
2	3	4	A	B	C	_	Input new character "C"
3	4	A	B	C	D	_	Input new character "D"

Ex2: I/D = "0", S = "1", Shift the display to the right.

1	2	3	4	_			Initial display
	1	2	3	4	A		Input new character "A"
		1	2	3	B	A	Input new character "B"
			1	2	C	B	Input new character "C"
				1	D	C	Input new character "D"

4. Display ON/OFF Control: (08H – 0FH)

The Display On / OFF Instruction is used to turn the display / Cursor / Blink ON / OFF. The controlling bits are D, C and B.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	C	B

D: Display On/Off bit

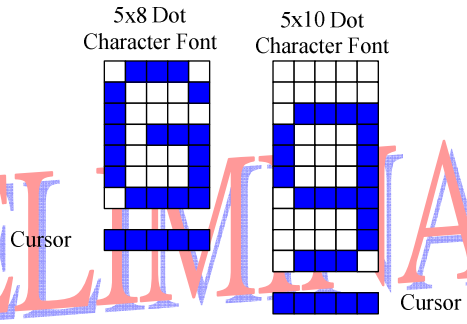
When D = "1", the entire display is turned ON.

When D = "0", the entire display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to "1". (POR)

C: Cursor Display Control bit

When C = "1", the cursor is displayed. In a 5 x 8 dot character font, the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line. (POR)

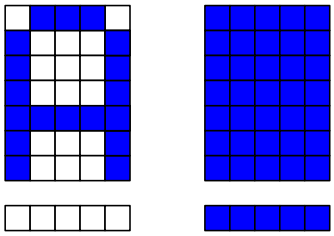
When C = "0", the cursor display is disabled. During a Display Data Write, the function of I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.



B: Cursor Blinking Control bit

When B = '0", the cursor character blink turn off. (POR)

When B = '1", the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250kHz. Please refer to the figure below.



Note: Figures 1 and 2 are alternately displayed

The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc.

5. Display/Cursor Shift:

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	S/C	R/L	*	*

*: Do not care (0 or 1)

S/C: Shift cursor to left or right

R/L: Shift display to left or right

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display data. Please refer to the table below.

In a 2-line Display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. The 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift. When S/L=0, the direction will reverse.

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC – 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

6. Function Set:

The Function Set Instruction has 4 controlling 5 bits, namely: DL, N, F and FT[1:0]. Please refer to the table below.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	NL	N	F	*	*

*: Do not care (0 or 1)

NL: Interface Data Length Control Bit

This is used to select the interface data length from 4-bit bus mode or 8-bit bus mode.

When DL= “1”, the data is sent or received in 8-bit length via the DB0 to DB7 (for an 8-Bit Data Transfer). (POR)

When DL= “0”, the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer). When the 4-bit data length is selected, the data must be sent or received twice.

N: Number of Display Line Bit

This is used to set the number of display lines.

When N = “1”, the 2-line display is selected.

When N = “0”, the 1-line display is selected. (POR)

F: Display Character Font Type Set

This is used to set the character font set.

When F = “0”, the 5 x 8 dot character font is selected. (POR)

When F = “1”, the 5 x 10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions other than the Busy Flag and Address Instruction. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

RESOL	N	F	No. of Display Lines	Character Font	Duty Factor
0	0	0	1	5×8 dots	1/8
0	0	1	1	5×10 dots	1/11
0	1	X	2	5×8 dots	1/16
1	0	0	2(Note1)	5×8 dots	1/32
1	0	1	2(Note2)	5×10 dots	1/22
1	1	X	4	5×8 dots	1/32

Note1: This case, the 1st DDRAM address is “00H~13H” and 2nd DDRAM address is “14H~27H”. And “COM1~COM8” output 1st line, “COM17~COM24” output 2nd line.

Note2: This case, the 1st DDRAM address is “00H~13H” and 2nd DDRAM address is “14H~27H”. And “COM1~COM11” output 1st line, “COM17~COM27” output 2nd line.

7. Character Generator RAM Address Set (Character Mode) or GDDRAM Page Address Set (Graphic Mode):

When select Character Mode (G/C=0), It sets Character Generator RAM Address ACG[5:0] to the Address Counter.

This instruction makes CGRAM data available from MPU.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ACG5	ACG4	ACG3	ACG2	ACG1	ACG0

Note: ACG is the CGRAM Address

When select graphic mode (Pad option G/C=1), It sets Page Address PAG to the Address Counter.

This instruction makes GDDRAM data available from MPU.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	PAG1	PAG0

PAG1	PAG0	Page Address
0	0	Page0 (POR)
0	1	Page1
1	0	Page2
1	1	Page3

Note: PAG is the Page Address

8. DDRAM Address Set (Character Mode) or GDDRAM Column Address Set (Graphic Mode):

When select Character Mode (G/C=0), this instruction is used to set the DDRAM Address binary ADD[6:0] into the Address Counter. The data is written to or read from the MPU for the DDRAM. If 1-line display is selected (N="0"), then ADD[6:0] can be 00H to 4FH. When the 2-line display is selected, then ADD[6:0] can be "00H" to "27H" for the first line and "40H" to "67H" for the second line. During writing and reading data, it defines cursor moving direction and shifts the display.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

Note:

(1)ADD = DDRAM Address

(2)The DDRAM address not used is forbidden to operation. When N = 0, the DDRAM address is 00H~4FH, the DDRAM address not used 50H~7FH is forbidden to write or read. When N = 1, the DDRAM address is 00H~27H and 40H~67H. The DDRAM Address not used 28H~3FH and 68H~7FH is forbidden to write or read.

When select Graphic Mode (G/C=0), this instruction is used to set the column address of display RAM. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 99 is accessed. The page address is not changed during this time.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1	CAD0

A7-A0 sets the column address of Graphic DDRAM.

D7	D6	D5	D4	D3	D2	D1	D0	Column address
1	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1	CAD0	
1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	2
1	0	0	0	0	0	1	0	3
1	0	0	0	0	0	1	1	4
1	0	0	0	0	1	0	0	5
.....								.....
1	1	0	1	1	1	1	1	96
1	1	1	0	0	0	0	0	97
1	1	1	0	0	0	0	1	98
1	1	1	0	0	0	1	0	99
1	1	1	0	0	0	1	1	100
11100100-11111111(0xE4-0xFF)								No Used

Note:

(1)CAD = Column Address

(2)The column address not used E4H~FFH is forbidden to write or read.

9. Busy Flag and Address Counter Read:

This instruction is used to read the Busy Flag (BF) to indicate if SH1111 is internally operating on a previously received instruction. If BF is set to "1", then the internal operation is in progress and the next instruction will not be accepted. If the BF is set to "0", then the previously received instruction has been executed and the next instruction can be accepted and processed. It is important to check the BF status before proceeding to the next write operation. The value of the Address Counter in binary AC[6:0] is simultaneously read out. This Address Counter is used by both the CGRAM and the DDRAM and its value is determined by the previous instruction. The contents of the address are the same as for the instructions – Set CGRAM Address and Set DDRAM Address.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Notes:

1. BF=Busy Flag

2. AC=Address Counter

10. Write Data to CGRAM / DDRAM / GDDRAM Instruction:

This instruction writes 8-bit binary data – Data[7:0] to the CGRAM or the DDRAM or the GDDRAM. The previous CGRAM or DDRAM or GDDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM or the GDDRAM. After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction. It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

11. Read Data from CGRAM / DDRAM / GDDRAM Instruction:

This instruction reads the 8-bit binary data – Data [7:0] from the CGRAM or the DDRAM or the GDDRAM. The Set CGRAM Address or Set DDRAM Address or Set GDDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

When the Read Instruction is executed in series, the next address data is normally read from the Second Read. There is no need for the Address Set Instruction to be performed before this Read instruction when using the Cursor Shift Instruction to shift the cursor (Reading the DDRAM). The Cursor Shift Instruction has the same operation as that of the Set the DDRAM Address Instruction.

After a Read instruction has been executed, the Entry Mode is automatically incremented or decremented by 1. It must be noted that regardless of the Entry Mode, the Display Shift is not executed.

After the Write instruction to either the CGRAM or DDRAM has been performed, the Address Counter is automatically increased or decreased by 1. The RAM data selected by the Address Counter cannot be read out at this time even if the Read Instructions are executed. Therefore, in order to correctly read the data, the following procedure has suggested:

1. Execute the Address Set or Cursor Shift (only with DDRAM) Instruction

2. Just before reading the desired data, execute the Read Instruction from the second time the Read Instruction has been sent.

12. Command Table2 Entry Instruction: (Double Bytes Command)

This instruction control the command table to command table2: (EFH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	1

Entry Command Table2 Sequence: (FAH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	1	0

This is a double bytes command. In order to enter command table2, user must send the following two commands together: 1st time sends command 0xEF, 2nd time sends command 0xFA.

The following example can enter command table2:

WriteCommand(0xEF);

WriteCommand(0xFA);

The following example can not enter command table2:

WriteCommand(0xEF);

WriteCommand(0xXX);

WriteCommand(0xFA);

Note: XX = select one data from ‘0’ ~ ‘F’

13. Command Table2 Exit Instruction: (Double Bytes Command)

This instruction control the command table back to command table1: (FEH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	0

Exit Command Table2 Sequence: (EBH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0

This is a double bytes command. In order to exit command table2, user must send the following two commands together: 1st time sends command 0xFE, 2nd time sends command 0xEB.

The following example can exit command table2:

WriteCommand(0xFE);

WriteCommand(0xEB);

The following example can not exit command table2:

WriteCommand(0xFE);

WriteCommand(0xXX);

WriteCommand(0xEB);

Note: XX = select one data from ‘0’ ~ ‘F’

14. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (10H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	0	0

■ Divide Ratio/Oscillator Frequency Data Set: (00H – FFH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_3 – A_0 defines the divide ration of the display clocks (DCLK).

When A[3:0] = 0000, Divide Ration = 2.

When A[3:0] ≠ 0000, Divide Ration = A[3:0]+1.

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	2
0	0	0	1	2(POR)
0	0	1	0	3
		:		:
1	1	1	1	16

A_7 – A_4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of fosc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	fosc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

15. Set Dis-charge / Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the Pre-charge/Discharge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Pre-charge / Dis-charge Period Mode Set: (20H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	0	0

■ Pre-charge/Dis-charge Period Data Set: (00H – FFH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Pre-charge Period Adjust: (A3 – A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	Note
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A_7 – A_4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Note:
When set A[3:0]=0, the period for display will increase 2 DCLKs. And there is no pre-charge period so that it will save power consumption.

16. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (30H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0

■ VCOM Deselect Level Data Set: (00H – FFH)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COMH} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.443	22H	0.648
03H	0.449	23H	0.655
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.732
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.545	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.597	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H – FFH	1		

17. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: I_{SEG} = α/256 X I_{REF} X scale factor

Where: α is contrast step; I_{REF} is reference current equals to 18.75μA; Scale factor = 16.

■ The Contrast Control Mode Set: (40H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

RS	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	0	0

■ Contrast Data Register Set: (00H – FFH)

By using this command to set eight bits of data to the contrast data register，the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

RS	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	0	0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	1	0	
0	0	:	:	:	:	:	:	:	:	:
0	0	1	0	0	0	0	0	0	0	80H
0	0	:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	1	0	
0	0	1	1	1	1	1	1	1	1	Large

18. VPP Voltage & Com/Segment Direction Set: (Double Bytes Command)

This instruction is used to set the VPP Voltage, Com/Segment data direction and DC-DC pump mode. (50H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	0	0	0

■ VPP Voltage & Com/Segment Direction Set:

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	CMS	SHL	0	DCS	VPP1	VPP0

VPP[1:0]: This two bits is used to set VPP voltage.

The voltage of VPP set refers to the table below.

VPP1	VPP0	VPP Voltage(V)
0	0	6.4
0	1	8.0
1	0	9.0
1	1	12.0 (POR)

DCS: This bit is used to select DC-DC pump mode.
When DCS = 0, Pump 3 times mode will be selected. (POR)
When DCS = 1, Pump 2 times mode will be selected.

SHL: This bit is used to set SEG direction.
When SHL = 0, the data direction is SEG1 -> SEG100 (POR)
When SHL = 1, the data direction is SEG100 -> SEG1

CMS: This bit is used to set COM direction.
When CMS = 0, the scan direction is COM1 -> COM32 (POR)
When CMS = 1, the scan direction is COM32 -> COM1

19. Graphic Vertical Scrolling: (Double Bytes Command)

This command is to set Graphic Vertical Scrolling (Graphic Mode Only).

■ Graphic Vertical Scrolling: (60H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	0	0	0

■ Graphic Vertical Scrolling:

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Vertical Scrolling				

■ Vertical Scrolling Control：This instruction setting the COM0 start point for the Vertical scrolling function. Sets the line address of display RAM to determine the starting Line. The RAM display data is displayed at the top row of LCD panel.

D4	D3	D2	D1	D0	Line address
0	0	0	0	0	1 (POR)
0	0	0	0	1	2
0	0	0	1	0	3
0	0	0	1	1	4
0	0	1	0	0	5
:	:	:	:	:	:
1	1	0	1	1	28
1	1	1	0	0	29
1	1	1	0	1	30
1	1	1	1	0	31
1	1	1	1	1	32

20. Graphic Duty Set: (Double Bytes Command)

This command is to set Graphic duty (Graphic Mode Only).

■ Graphic Duty Set: (70H)

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	0

■ Graphic Duty Set:

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	Graphic Duty			

■ Graphic Duty Select Instruction (Graphic Mode Only). This instruction controls the COM duty selection.

SH1111 support 9 duty types in Graphic mode. Each of these modes will control the number of multi COM drive. Please refer the table as bellow.

D[3:0]	Duty	Function
0	1/1	All com always on
1	1/2	The Grouping is COM1~16 and COM17~32
2	1/3	The Grouping is COM1~10, COM11~20 and COM21~32
3	1/4	The Grouping is COM1~8, COM9~16, COM17~24 and COM25~32
4	1/5	The Grouping is COM1~6, COM7~12, COM13~18, COM19~24 and COM25~32
5	1/6	The Grouping is COM1~5, COM6~10, COM11~15, COM16~20, COM21~25 and COM26~32
6	1/7	The Grouping is COM1~4, COM5~8, COM9~12, COM13~16, COM17~20, Com21~24 and COM25~32
7	1/8	The Grouping is COM1~4, COM5~8, COM9~12, COM13~16, COM17~20, COM21~24, COM25~28 and COM29~32
8	1/16	The Grouping is COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12, COM13~14, COM15~16, COM17~COM18, COM19~COM20, COM21~COM22, COM23~COM24, COM25~COM26, COM27~COM28, COM29~COM30 and COM31~COM32
9	1/32	Normal display (POR)
10~15	1/32	Normal display

21. Font Table & Cursor Blinking Duty Control Set: (Double Bytes Command)

This command is used to control the font table and cursor blinking duty.

■ Font Table & Cursor Blinking Duty Control Register: (80H)

When this command is input, the font table & cursor blinking control register command becomes enabled. Once the font table & cursor blinking control mode has been set, no other command except for the font table control & cursor blinking register command can be used. Once the font table & cursor blinking data set command has been used to set data into the register, then the font table & cursor blinking control mode is released.

RS	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	0

■ Font Table Enable & Font Table Selection & Cursor Blinking Duty Set:

RS	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	BD2	BD1	BD0	0	FTE	FTS1	FTS0

FTE: Software Font Table Set Enable Bit.

When FTE = 0, software font table set function disable. The font table is selected by pad option FT[1:0]. (POR)

When FTE = 1, software font table set function enable. The font table is selected by register option FTS[1:0]. At the same time, the font select by pad option FT[1:0] is invalid.

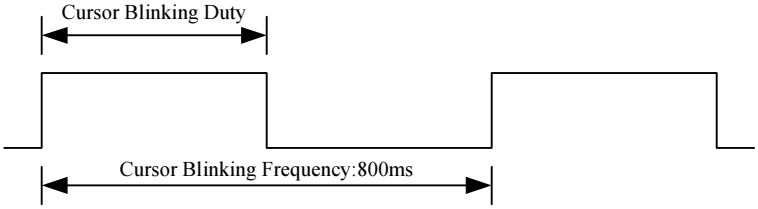
FTS [1:0]: Software Font Table Selection Control Bit.

FTS1	FTS0	Font Table
0	0	ENGLISH_JAPANESE CHARACTER FONT TABLE(POR)
0	1	WESTERN EUROPEAN CHARACTER FONT TABLE-I
1	0	ENGLISH_RUSSIAN CHARACTER FONT TABLE
1	1	WESTERN EUROPEAN CHARACTER FONT TABLE-II

BD[2:0]: Cursor Blinking Duty Selection.

These three bits are used to select one Blinking duty out of the four for further process.

D2	D1	D0	Cursor Blinking Duty
0	0	0	400ms
0	0	1	350ms
0	1	0	300ms(POR)
0	1	1	250ms
1	0	0	200ms
1	0	1	150ms
1	1	0	100ms
1	1	1	50ms



21. SH1111 ID Read:

This instruction is used to read the SH1111 ID.

RS	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	ON/OFF	ID					

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID：These bits contain the information of the chip. They output bits 010001(it means 11H).

Command Table 1

Command	Code										Function
	RS	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1. Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area. (POR = 01H), ▲
2. Display/ Cursor Home	0	0	0	0	0	0	0	0	1	*	Counter with DDRAM address 00H. (POR = 10H), ▲●
3. Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write). (POR = 06H), ▲
4. Display ON/OFF	0	0	0	0	0	0	1	D ▲ ●	C ▲	B ▲	Specify activation of display (D) cursor and blinking of character at cursor position (B). (POR = 08H),
5. Display/Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.
6. Function Set	0	0	0	0	1	DL	N	F	*	*	Set number of display line (N), and character font (F). (POR = 30H), ▲
7. CGRAM Address Set (GC=0, Character Mode Only)	0	0	0	1	ACG						Load the address counter with a CG RAM address. Subsequent data access is for CG RAM data. (POR = 00H), ▲
or Page Address Set (GC=1, Graphic Mode Only)	0	0	0	1	0	0	0	0	PAG[1:0]		Set Page Address of GDDRAM. (POR = 00H), ●
8. DD RAM Address Set (GC=0, Character Mode Only)	0	0	1	ADD[6:0]							Load the address counter with a DDRAM address. Subsequent data access is for DD RAM data. (POR = 00H), ▲
or Column Address Set (GC=1, Graphic Mode Only)	0	0	1	CAD[6:0]							Set Column Address of GDDRAM. (POR = 00H), ●
9. Busy Flag & Address Counter Read	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read Busy Flag (BF) and Address Counter (POR = 00H), ▲●
10. CG RAM/ DD RAM/ GDDRAM Data Write	1	0	Write Dada								Write data to CG RAM or DD RAM or GDDRAM. (POR = 00H), ▲●
11. CG RAM/ DD RAM/ GDDRAM Data Read	1	1	Read Data								Read data from CG RAM or DD RAM or GDDRAM. (POR = 00H), ▲●

Entry or Exit Extend Command Table2 Sequence:

12. Enter Extend Command Table2	0	0	1	1	1	0	1	1	1	1	Enter extend Command Table2 mode. (POR = EFH), ▲●
	0	0	1	1	1	1	1	0	1	0	Entry Sequence (POR = FAH), ▲●
13. Exit Extend Command Table2	0	0	1	1	1	1	1	1	1	0	Exit from extend Command Table2. (POR = FEH), ▲●
	0	0	1	1	1	0	1	0	1	1	Exit Sequence (POR = EBH), ▲●

Command Table 2 (Continued)

Command	Code										Function
	RS	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
14. Divide Ratio/Oscillator Frequency Data Set	0	0	0	0	0	1	0	0	0	0	Double Byte command: Set the frequency of the internal display clocks. (POR = 51H), ▲●
			Oscillator Frequency				Divide Ratio				
15. Dis-charge /Pre-charge Period Mode Set	0	0	0	0	1	0	0	0	0	0	Double Byte command: Set the duration of the Dis-charge and Pre-charge period. (PDCVS = 0, POR = 22H; PDCVS = 1,POR = FFH), ▲●
			Dis-charge Period				Pre-charge Period				
16. VCOM Deselect Level Data Set	0	0	0	0	1	1	0	0	0	0	Double Byte command: Set the Common pad output voltage level at deselect stage. (PDCVS = 0, POR = 35H; PDCVS = 1, POR = 40H), ▲●
			VCOM								
17. Segment Contrast Out Level	0	0	0	1	0	0	0	0	0	0	Double Byte command: Set Segment Contrast out level (PDCVS=0, POR = 80H; PDCVS=1, POR = FFH), ▲●
	0	0	CT(=BVR)								
18. VPP & Com/Segment Direction Set	0	0	0	1	0	1	0	0	0	0	Double Byte command: (POR = 03H), ▲●
	0	0	0	0	CMS	SHL	0	DCS	VPP[1:0]		
19. Graphic Vertical scrolling set	0	0	0	1	1	0	0	0	0	0	Double Byte command: Set Graphic Vertical scrolling. (POR = 00H), ●
	0	0	0	0	0	Graphic Vertical scrolling					
20. Graphic duty set	0	0	0	1	1	1	0	0	0	0	Double Byte command: Set Graphic duty. (POR = 09H), ●
	0	0	0	0	0	0	Graphic duty				
21. Font Table & Cursor Blinking Duty Control Set	0	0	1	0	0	0	0	0	0	0	Double Byte command: (POR = 20H), ▲
	0	0	0	BD[2:0]			0	FTE	FTS[1:0]		
22. Read SH1111 ID	0	1	0	ON/OFF	ID						Return ID : 010001 (11H), ▲●

Note:

1. ▲ = Character Mode Effective, ● = Graphic Mode Effective
2. Do not use any others command, otherwise it will cause system malfunction.

Operation Example

1. 8-bit Operation and 8-Digit 1-line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power On. (SH1111 starts initializing)		Power On Reset. No Display.
2	Function Set. RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 * *		Set to 8-bit operation and select 1-line display line and character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0	_	Display On. Cursor appear.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DDRAM / CGRAM. Now the display has no shift.
5	Write data to CGRAM / DDRAM. 1 0 0 1 0 1 0 1 1 1	W_	Write “W”. The cursor is increased by one and shift to the right.
6	Write data to CGRAM / DDRAM. 1 0 0 1 0 0 0 1 0 1	WE_	Write “E”. The cursor is increased by one and shift to the right.
7	……	……	……
8	Write data to CGRAM / DDRAM. 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write “E”. The cursor is increased by one and shift to the right.
9	Entry Mode Set. 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing.
10	Write data to CGRAM / DDRAM. 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write “ “ (Space) The cursor is increased by one and shift to the right.
11	Write data to CGRAM / DDRAM. 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write “C“ The cursor is increased by one and shift to the right.
12	……	……	……
13	Write data to CGRAM / DDRAM. 1 0 0 1 0 0 0 0 1 1	COMPAMY_	Write “Y“ The cursor is increased by one and shift to the right.
14	Cursor or display shift. 0 0 0 0 0 1 0 0 * *	COMPAMY	Only shift the cursor’s position to the left (Y).
15	Cursor or display shift. 0 0 0 0 0 1 0 0 * *	COMPAMY	Only shift the cursor’s position to the left (M).
16	Write data to CGRAM / DDRAM. 0 0 0 0 0 1 0 0 * *	OMPANY	Write “N“ The display moves to the left.
17	Cursor or display shift. 0 0 0 0 0 1 1 1 * *	COMPANY_	Shift the display and the cursor’s position to the right.
18	Cursor or display shift. 0 0 0 0 0 1 0 1 * *	OMPANY_	Shift the display and the cursor’s position to the right.
19	Write data to CGRAM / DDRAM. 0 0 0 0 0 1 0 0 * *	COMPANY _	Write “ ”(Space) The cursor is increased by one and shift to the right.
20	……	……	……
21	Return home. 0 0 0 0 0 0 0 0 1 0	WELCOME_	Both the display and the cursor return to the original position (address 0).

2. 4-bit Operation and 8-Digit 1-line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power On. (SH1111 starts initializing)		Power On Reset. No Display.
2	Function Set. RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	0 0 0 0 0 0 0 0 0 0 * *		Set to 4-bit operation and select 1-line display and character font.
4	0 0 0 0 0 0 0 0 1 1 1 0	_	Display On. Cursor appears.
5	0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DDRAM / CGRAM. Now the display has no shift.
6	1 0 0 1 0 1 1 0 0 1 1 1	W_	Write “W”. The cursor is increased by one and shift to the right.

3. 8-bit Operation and 8-Digit 2-line Display (Using Internal Reset)

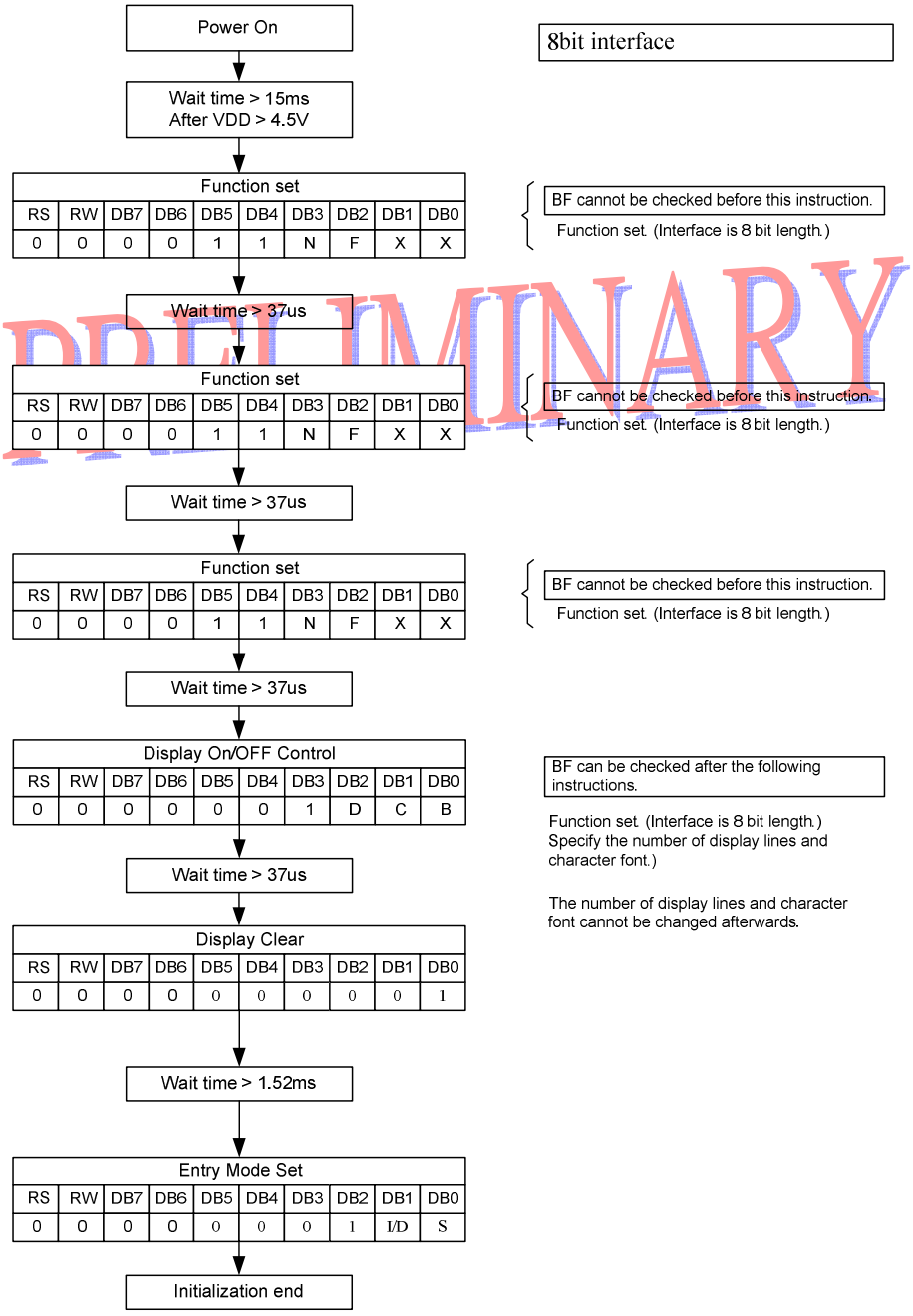
No.	Instruction	Display	Operation
1	Power On. (SH1111 starts initializing)		Power On Reset. No Display.
2	Function Set. RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 * *		Set to 8-bit operation and select 2-line display line and 5×8 dot character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0	_	Display On. Cursor appear.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DDRAM / CGRAM. Now the display has no shift.
5	Write data to CGRAM / DDRAM. 1 0 0 1 0 1 0 1 1 1	W_	Write “W”. The cursor is increased by one and shift to the right.
6	.....	.....	.....
7	Write data to CGRAM / DDRAM. 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write “E”. The cursor is increased by one and shift to the right.
8	Set DDRAM address. 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets the DDRAM’s address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CGRAM / DDRAM. 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write “T“. The cursor is increased by one and shift to the right.
10	.....	.....	.....
11	Write data to CGRAM / DDRAM. 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write “T“ The cursor is increased by one and shift to the right.
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	WELCOME TO PARTY_	When writing, it sets mode for the display shift.
13	Write data to CGRAM / DDRAM. 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write “Y“. The cursor is increased by one and shift to the right.
14	.....	.....	.....
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

Power On/Off Sequence

1. 8 bit interface: When user set IM[2:0] the following combinations.

IM2	IM1	IM0	MPU Interface
0	0	0	8-bit 6800
0	0	1	8-bit 8080
0	1	0	4-wire SPI
0	1	1	IIC
1	1	0	3-wire SPI
1	1	1	IIC

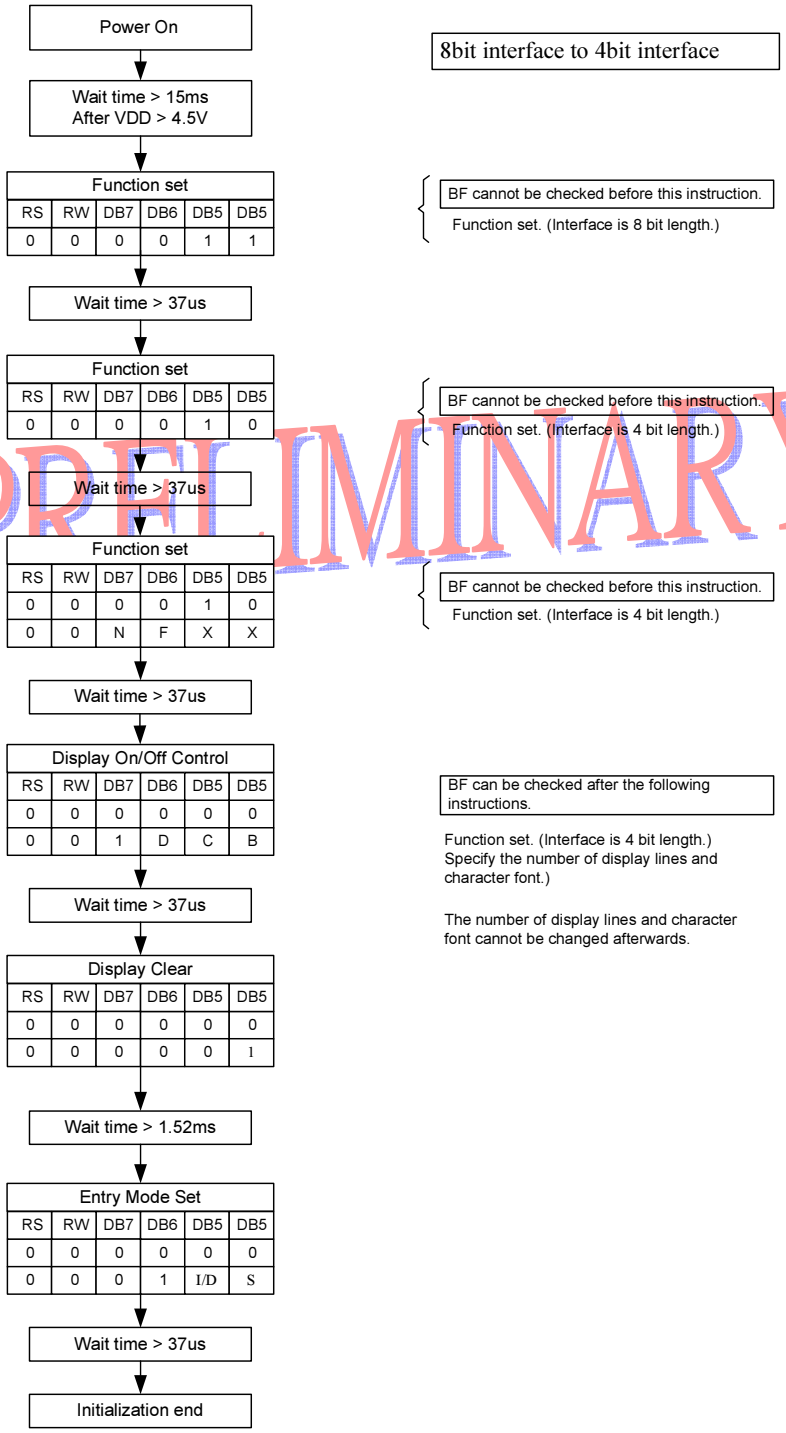
After power on, SH1111 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows.



2. 8 bit interface to 4bit interface: when user set IM[2:0]=000 to select 8bit 6800 interface, user can set command6 “NL=0” to select 4bit 6800 interface (when user set IM[2:0]=001 to select 8bit 8080 interface, user can set command6 “NL=0” to select 4bit 8080 interface).

IM2	IM1	IM0	MPU Interface
0	0	0	8-bit 6800
0	0	1	8-bit 8080

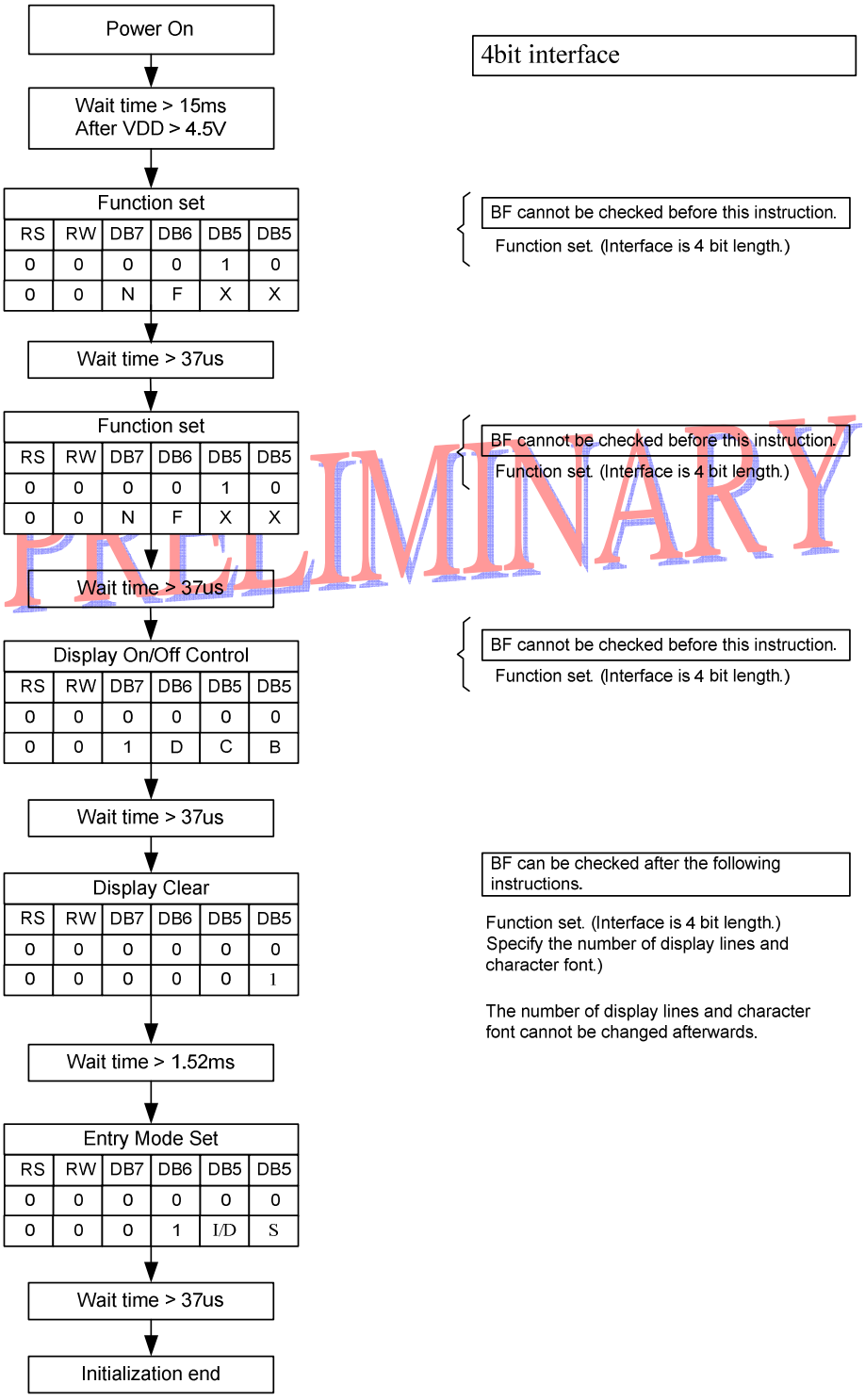
After power on, SH1111 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows.



3. 4bit interface: when user set IM[2:0]=100 to select 4bit 6800 interface or set IM[2:0]=101 to select 4bit 8080 interface.

IM2	IM1	IM0	MPU Interface
1	0	0	4-bit 6800
1	0	1	4-bit 8080

After power on, SH1111 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows.



Absolute Maximum Rating*

DC Supply Voltage (VDD1)……-0.3V to +5.6V

DC Supply Voltage (VDD2)…… -0.3V to +5.6V

DC Supply Voltage (V_{PP})…… -0.3V to +14.5V

Input Voltage…… -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature …… -40°C to +85°C

Storage Temperature …… -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (**GND** = 0V, V_{DD1} =3.5V – 5.5V, V_{DD2} = 2.7V – 5.5V, T_A = +25°C, unless otherwise specified)

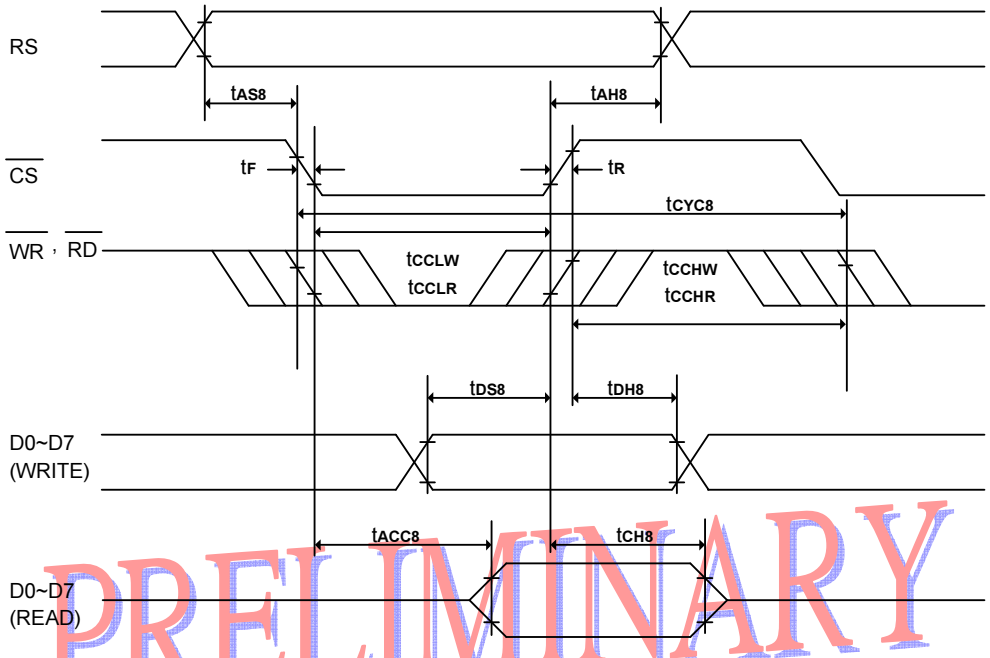
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Power supply of I/O	3.5	-	5.5	V	For 5V system
V_{DD2}	Power supply of logic device	2.7	-	5.5	V	
V_{PP}	OLED Operating voltage	5.0	-	14.0	V	
I_{DD1}	Dynamic current Consumption 1 in V_{DD1}	-	110	160	µA	V_{DD1} = V_{DD2} =5V, I_{REF}=18.75µA, BVR = 11111111(FFH), Internal charge pump OFF(VPPS=0), Display ON, display data = All ON, No panel attached.
I_{DD2}	Dynamic current Consumption 2 in V_{DD1} & V_{DD2}	-	3.5	4	mA	V_{DD1} = V_{DD2} =5V, I_{REF}=18.75µA, BVR = 11111111(FFH), Internal charge pump ON(VPPS=1), Display ON, Display data = All ON, No panel attached.
I_{PP}	OLED dynamic current consumption in V_{PP}	-	1.8	2.54	mA	V_{DD1} = V_{DD2} = 5v, VPP =12V(external, VPPS=0), BVR = 11111111(FFH), Display ON, Display data = All ON, No panel attached.
I_{SP}	Sleep mode current Consumption in V_{DD1} & V_{DD2}	-	-	10	µA	During sleep, T_A = +25°C, V_{DD1} = 5V, V_{DD2} = 5V, (Internal VPP,VPPS=1)
	Sleep mode current Consumption in V_{PP}	-	-	10	µA	During sleep, TA = +25°C, VPP = 12v (external, VPPS=0)
I_{SEG}	Segment output current	-	-600	-	µA	V_{DD1} = 5v, V_{PP} = 12v, R_{LOAD} = 20kΩ, Display ON. BVR=11111111(FFH)
ΔI_{SEG1}	Segment output current uniformity	-	-	±5	%	ΔI_{SEG1} = (I_{SEG} – I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [1:100] at BVR=11111111(FFH)
ΔI_{SEG2}	Adjacent segment output Current uniformity	-	-	±5	%	ΔI_{SEG2} = (I_{SEG}[N] – I_{SEG}[N+1])/(I_{SEG}[N] + I_{SEG}[N+1]) X 100% I_{SEG} [1:100] at BVR=11111111(FFH)

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.7 X V_{DD1}	-	V_{DD1}	V	RS, D0 – D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0, IM1, IM2, VDD1_OPT and $\overline{RES}$
V_{ILC}	Low-level input voltage	GND	-	0.3 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.7 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 – D7, and CL)
V_{OLC}	Low –level output voltage	GND	-	0.3 X V_{DD1}	V	I_{OL} = 0.5mA (D0 – D7, and CL)
V_{OLCS}	SDA low –level output voltage	GND	-	0.3 X V_{DD1}	V	VDD1<2V, I_{OL}=2mA (SDA)
				0.4		VDD1 ≥ 2V, I_{OL}=3mA (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or GND (RS, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0, IM1, IM2, VDD1_OPT and $\overline{RES}$)
I_{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 – D7, and CL are in high impedance
f_{OSC}	Oscillation frequency	-	400	-	KHz	T_A = +25°C
f_{FRM}	Frame frequency for 16 Commons	-	116	-	Hz	When f_{OSC} = 400KHz, Divide ratio = 2, Common width = 54 DCLKs (Discharge = 2 DCLKs, Precharge = 2 DCLKs)

AC Characteristics

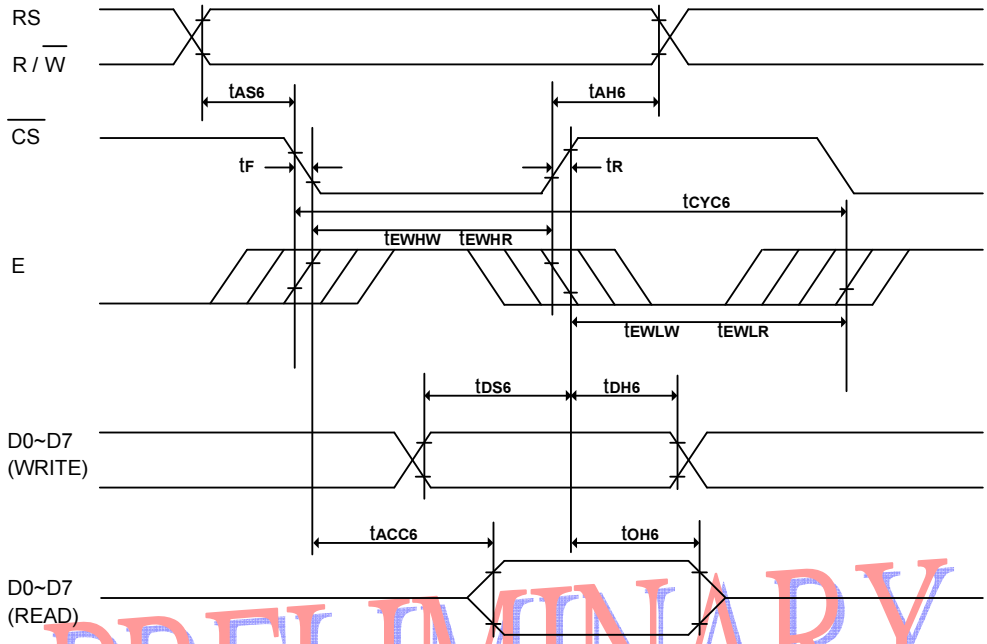
(1) System buses Read/Write characteristics 1 (For the 4/8 bit 8080 Series Interface MPU)



(V_{DD1} = 2.2 – 5.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	500	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	66	-	-	ns	
t_{DH8}	Data hold time	25	-	-	ns	
t_{CH8}	Output disable time	16	-	110	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	230	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	166	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	200	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	166	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	166	-	-	ns	
t_R	Rise time	-	-	25	ns	
t_F	Fall time	-	-	25	ns	

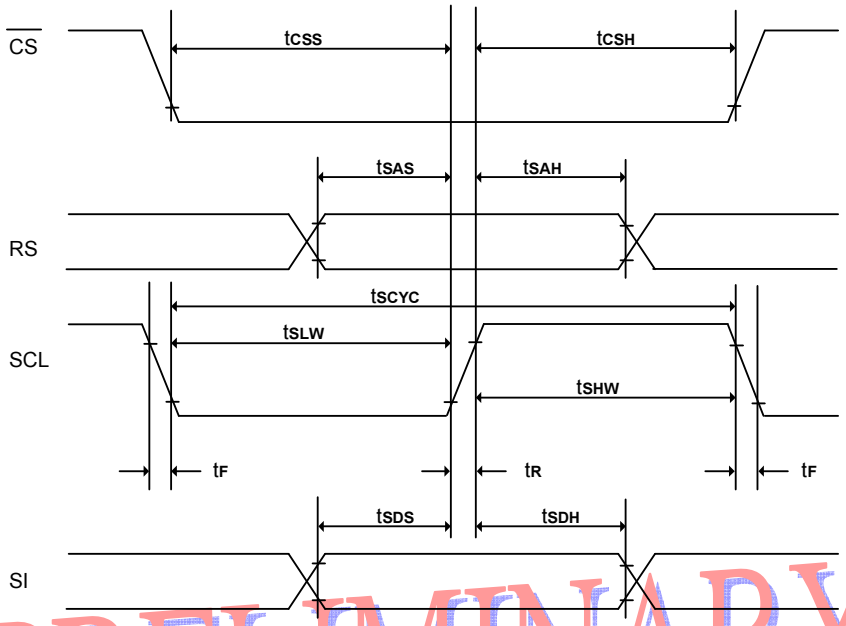
(2)System buses System buses Read/Write Characteristics 2 (For the 4/8 bit 6800 Series Interface MPU)



(V_{DD1} = 2.2 – 5.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	500	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	66	-	-	ns	
t_{DH6}	Data hold time	25	-	-	ns	
t_{OH6}	Output disable time	16	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	166	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	200	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	166	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	166	-	-	ns	
t_R	Rise time	-	-	25	ns	
t_F	Fall time	-	-	25	ns	

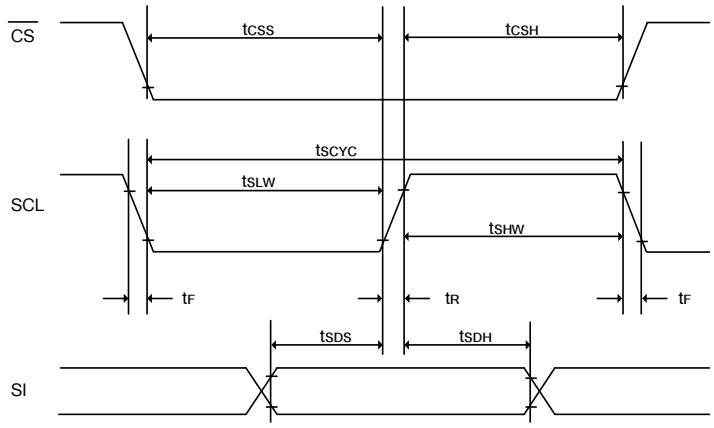
(3)System buses Write characteristics 3 (For 4 wire SPI)



(V_{DD1} = 2.2 – 5.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

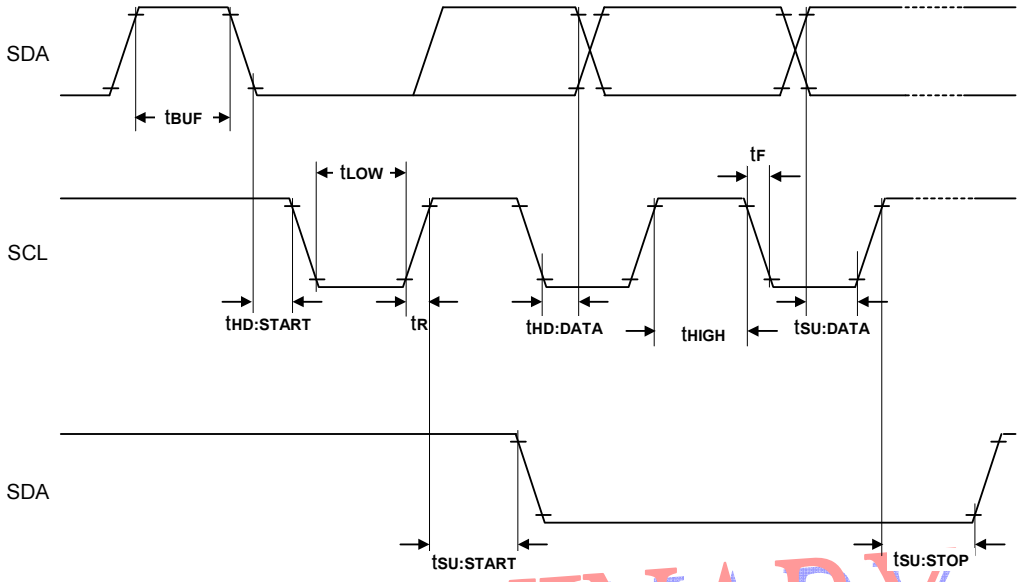
(4)System buses Write characteristics 4(For 3 wire SPI)



(V_{DD1} = 2.2 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

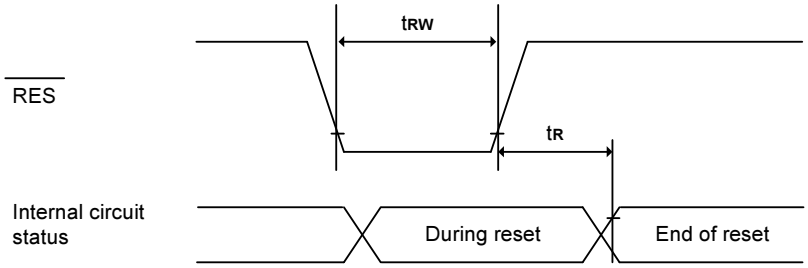
(5)I²C interface characteristics



(V_{DD1} = 2.2 – 5.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	uS	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	uS	
$T_{SU:DATA}$	data setup time	100	-	-	nS	
$T_{HD:DATA}$	data hold time	0	-	0.9	uS	
T_R	SCL，SDA rise time	20+0.1Cb	-	300	nS	
T_F	SCL，SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	uS	
$T_{HD:START}$	START Hold time	0.6	-	-	uS	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	uS	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	uS	

(6)Reset Timing



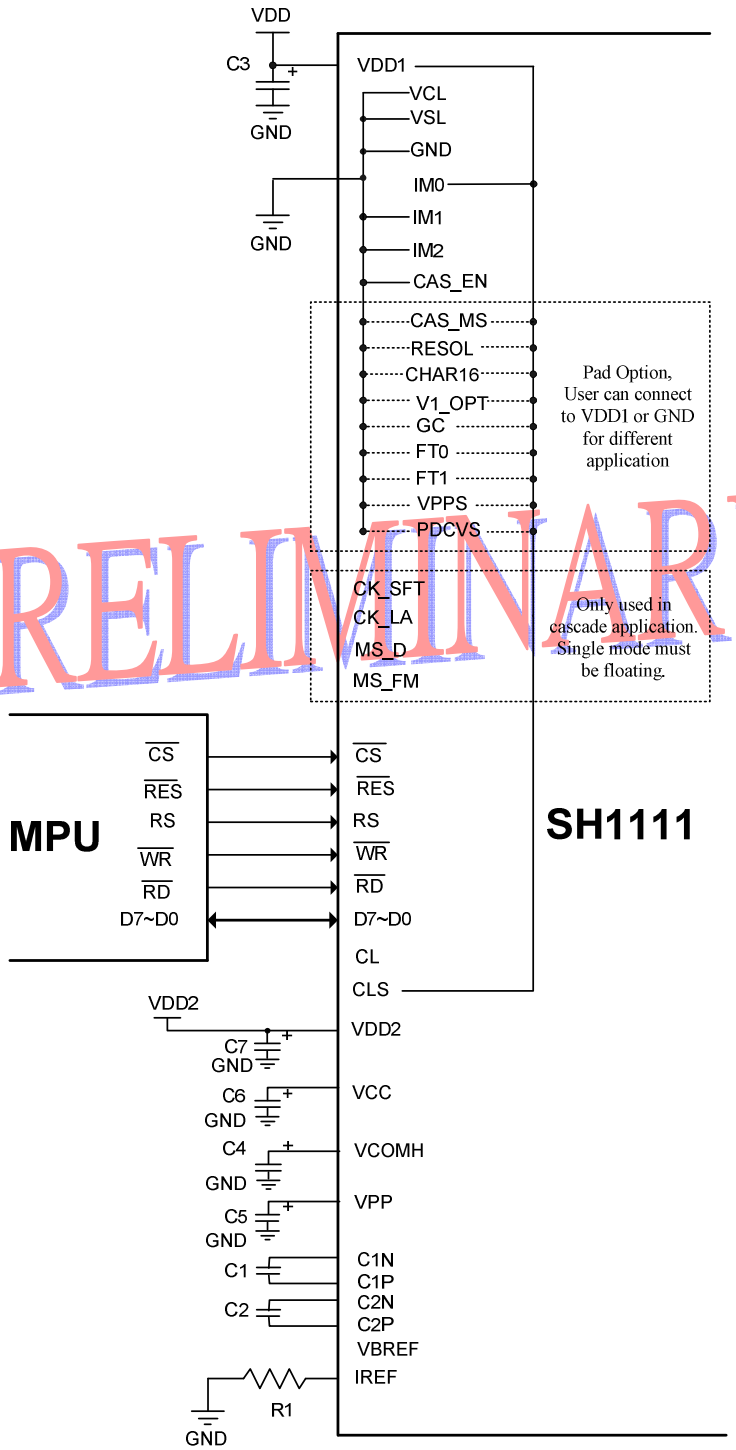
(V_{DD1} = 2.2 – 5.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	

Application Circuit (for reference only)

Reference Connection to MPU:

1. 8-bit 8080 Series Interface: (Internal Oscillator, Build-in DC-DC)

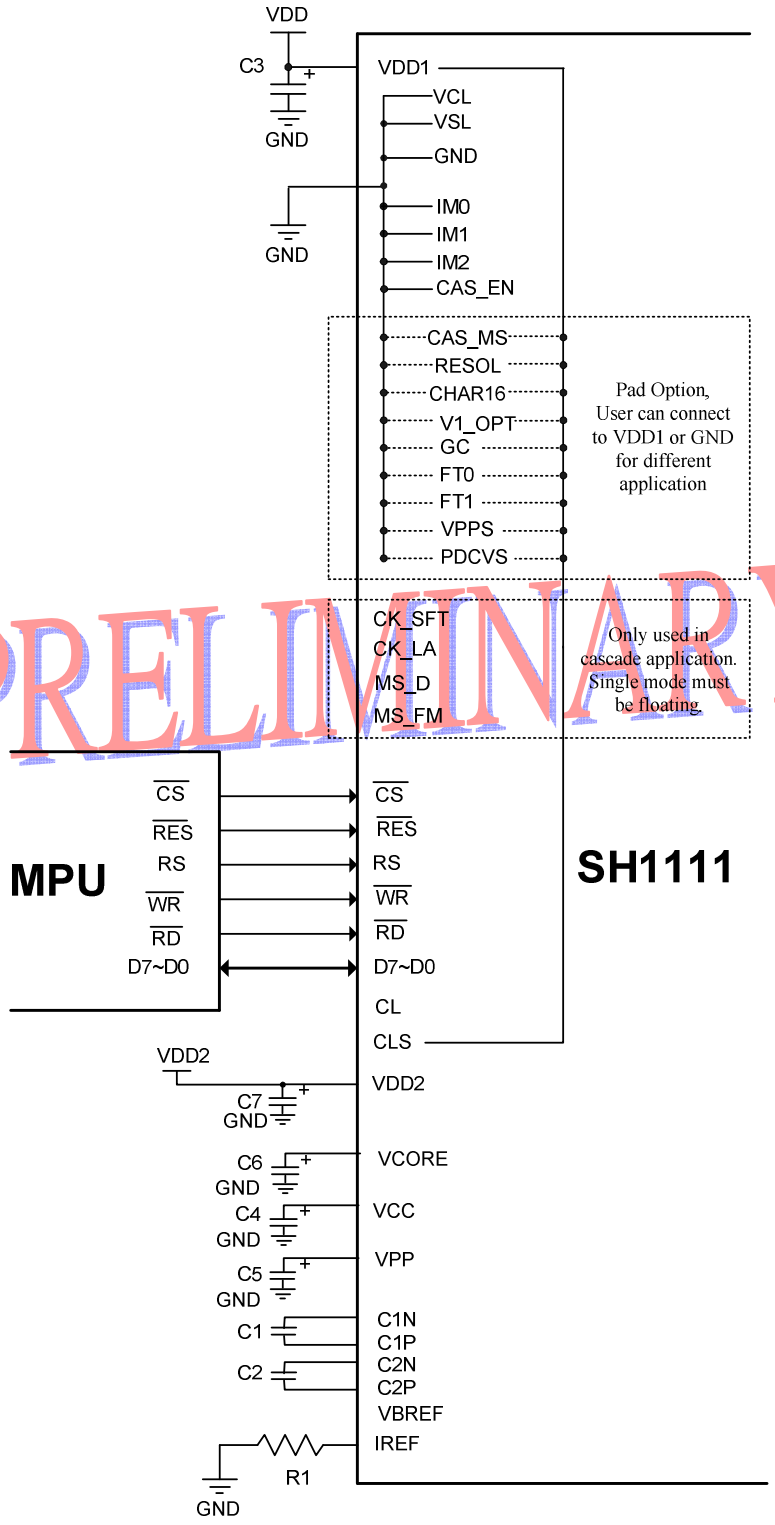


Note:

C_3 – C_5, C_6, C_7: 4.7μF. C_1, C_2: 1μF

R1: about 480k(I_{SEG}=300uA), R_1 = (Voltage at I_{REF} – GND)/I_{REF}

2. 8-bit 6800 Series Interface: (Internal Oscillator, Built-in DC-DC)

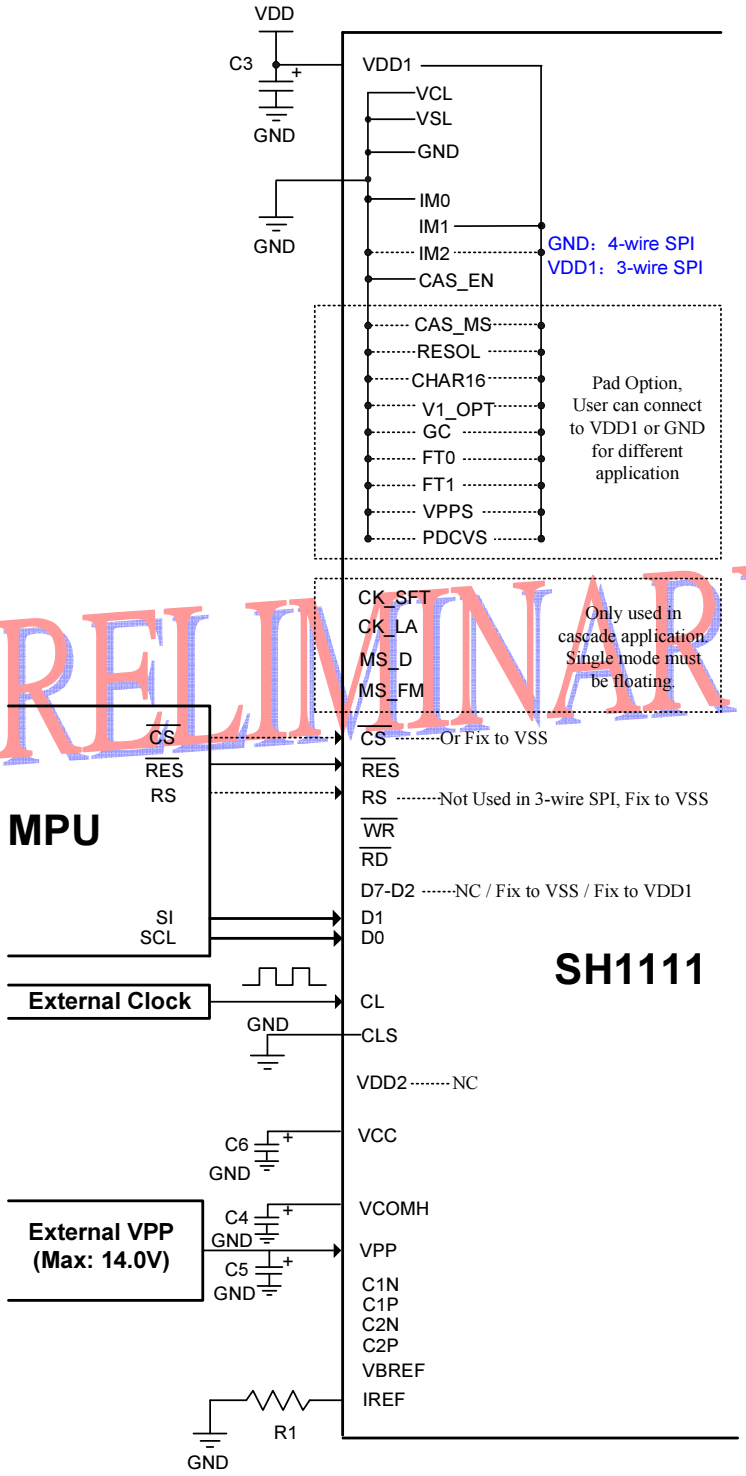


Note:

C_3 – C_5, C_6, C_7: 4.7μF. C_1, C_2 : 1μF

R1: about 480k(I_{SEG}=300uA), R_1 = (Voltage at I_{REF} – GND)/I_{REF}

3. Serial Interface (3-wire or 4-wire SPI): (External Oscillator, External VPP, Max 14.0V)



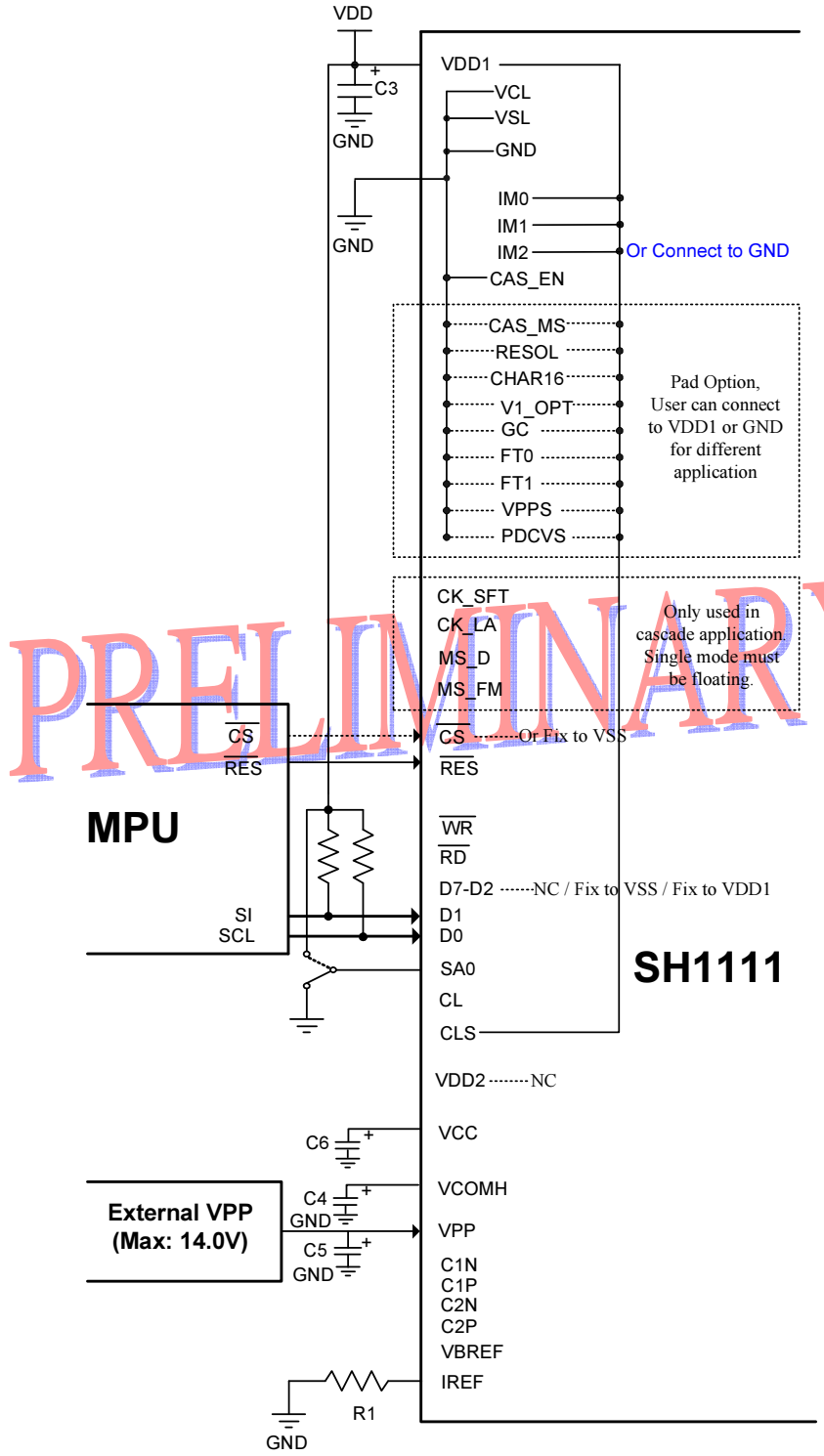
$C_3 - C_5$, C_6: 4.7μF

R1: about 480k(I_{SEG}=300uA), R_1 = (Voltage at I_{REF} – GND)/I_{REF}

$\overline{WR}$ and $\overline{RD}$ are not used in SPI mode, should fix to GND or VDD1.

$\overline{CS}$ can fix to GND in SPI mode.

4. I²C Interface: (Internal oscillator, External VPP, Max 14.0V)



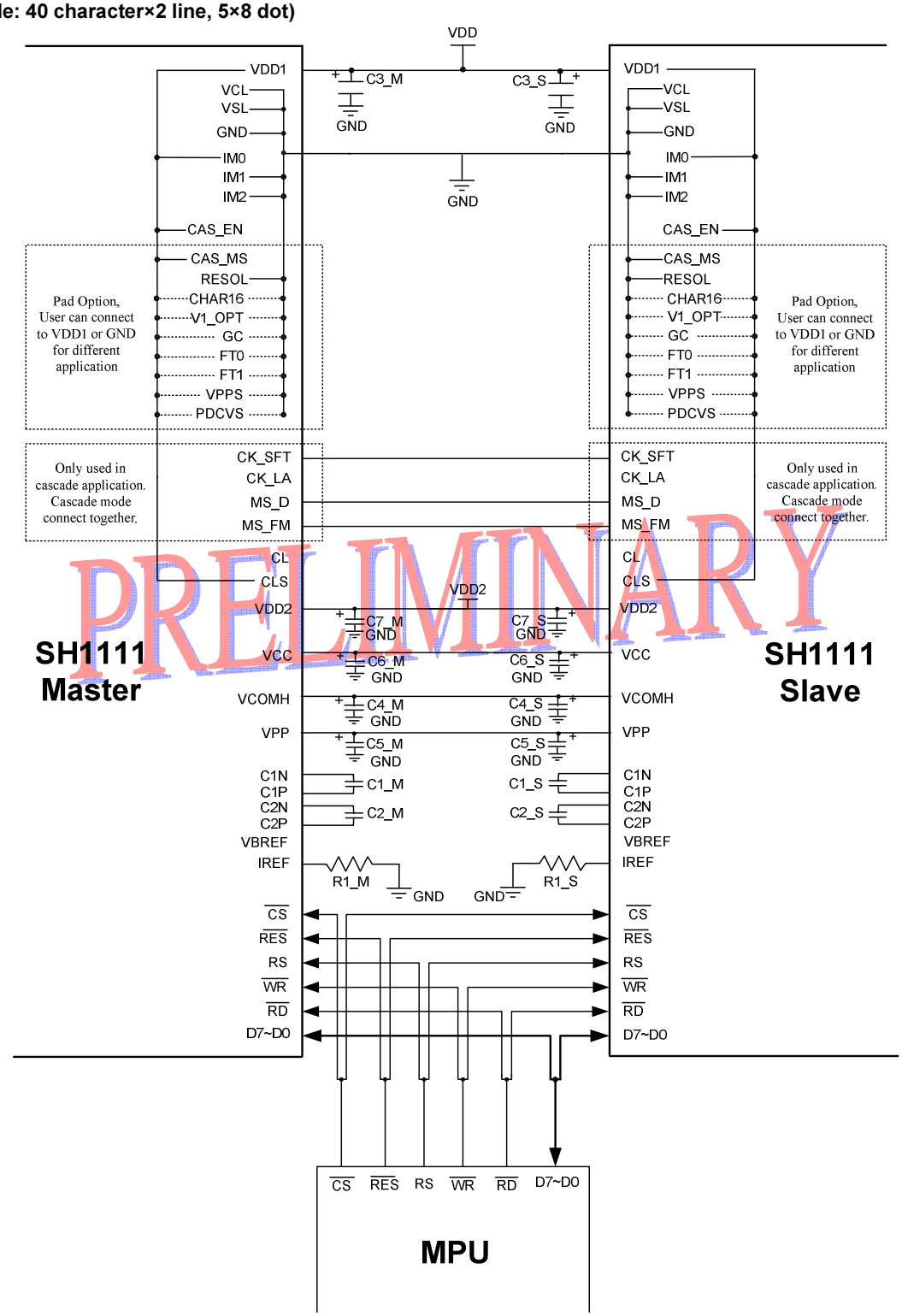
$C_3 - C_5$, C_6: 4.7μF

R1: about 480k(I_{SEG}=300uA), R_1 = (Voltage at I_{REF} – GND)/I_{REF}

$\overline{WR}$ and $\overline{RD}$ are not used in IIC mode, should fix to GND or VDD1.

$\overline{CS}$ can fix to GND in IIC mode.

5. Cascade Application: 8-bit 8080 Series Interface, Internal Oscillator, Build-in DC- DC (Example: 40 character×2 line, 5×8 dot)



Note:
M = Master, S = Slave.
C3 – C5, C6, C7: 4.7μF, C1, C2: 1μF
R1: about 480k(I_{SEG}=300uA) , R1 = (Voltage at IREF – GND)/IREF

Package Information

Ordering Information

Part No.	Package
SH1111G-BD001	Gold bump on chip tray

Spec Revision History

Version	Content	Date
V0.0	Original	2014.12.10
V0.1	1. Modify “VSL”, “CK_LA” Pad definition. (Page3) 2. Modify COM Pad pitch to 46um. (Page7) 3. Modify Pad location. (Page8) 4. Modify the 4bit 6800-series Parallel Interface timing. (Page10) 5. Added description of 1601 and 1604 note. (Page17) 6. Added DDRAM Address description of “5×8 dot Font” or “5×10 dot Font”. (Page 17~20) 7. Modify Master and Slave definition. (Page35,36,39) 8. Modify “4bit interface” and added “8bit interface to 4bit interface”. (Page70~71) 9. Modify DC Characteristics.(Page72)	2015.02.06
V0.2	1. Modify GND Pad number. (Page3) 2. Modify Ordering Information. (Page85) 3. Modify “I_{REF} is reference current equals to 18.75μA; Scale factor = 16”. (Page58)	2015.03.25
V0.2_1	1. Modify DC Character of IDD2 Value. (Page72) 2. Modify Iref Res R1 Value: 480K. (Page80~84)	2015.04.14